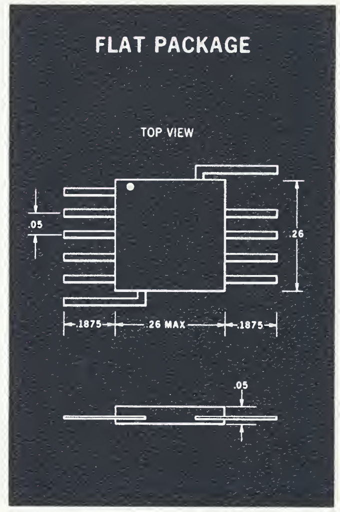
DTμL 931 CLOCKED FLIP-FLOP

FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION - The Fairchild Diode-Transistor Clocked Flip-Flop is one of a set of compatible, integrated, logic building blocks designed for low-power and high immunity to noise from -55°C to +125°C. Other DTμL elements are the 930 Dual Gate, the 932 Buffer, and 933 Input Extender.

The 931 Clocked Flip-Flop features an AND gate input permitting operation in either the R-S or J-K mode. The 931 element consists of two flip-flops connected as a "master-slave" combination, thus eliminating the need for capacitors or other circuit delay elements. The "master" flip-flop stores the input information when the clock voltage is high and transfers it to the "slave" when the clock voltage is low. Direct (unclocked) set and clear inputs are also provided.

For complete test conditions and limits, refer to DTμL Composite specification. Refer also to specifications on DTμL 930 Dual Gate, DTμL 932 Dual Buffer, DTμL 933 Dual Extender, DTμL 944 Dual Power Gate, and DTμL 946 Quad Gate.



R-S MODE TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Undetermined

X - Either a one or a zero can be present

"1" more positive than "0"

For J-K Mode Operation: Connect S_1 to $\overline{Q}$ and C_1 to Q

J-K MODE TRUTH TABLE

t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

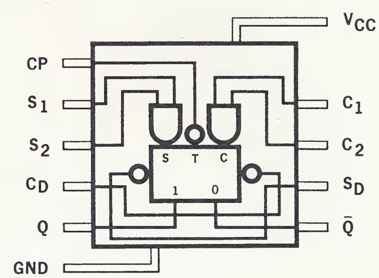
"1" more positive than "0"

For J-K Mode Operation:

Connect S_2 to $\overline{Q}$ and

C_2 to Q

FLAT PACKAGE



(Top View)

Input Load Factor *

CP	2
S_1, S_2, C_1, C_2	2/3

* DTμL 930 Dual Gate Input = 1

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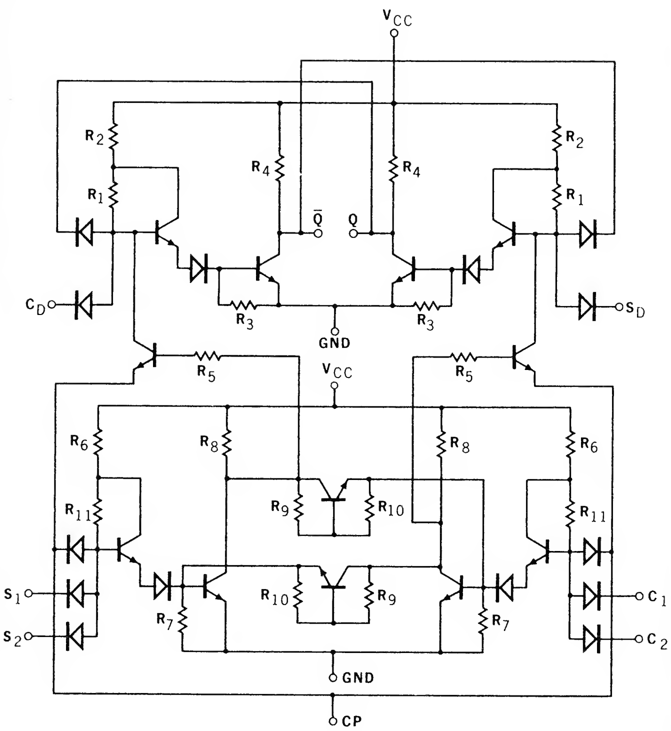
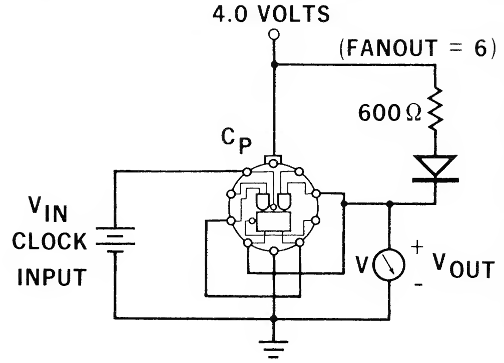
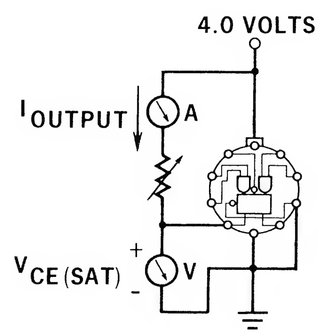
SCHEMATIC DIAGRAM OF 931 ELEMENT



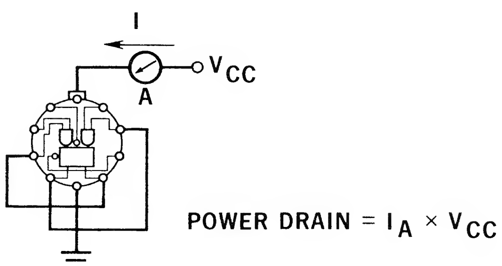
TEST CONDITIONS FOR FIGURES 1, 2, 3



TEST CONDITIONS FOR FIGURE 4

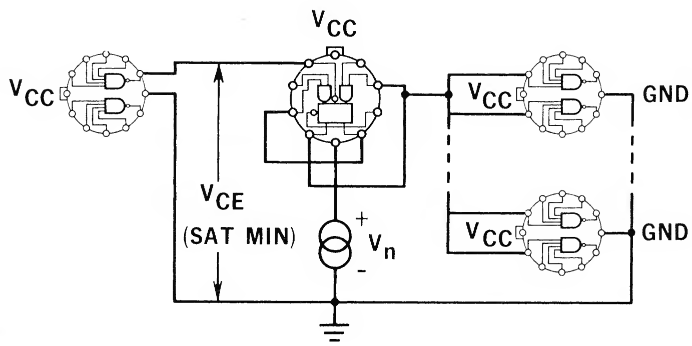


TEST CONDITIONS FOR FIGURE 5



POWER DRAIN = $I_A \times V_{CC}$

TEST CONDITIONS FOR FIGURES 6, 7, 8, 9



1. Refer to Fig. A. The "master" flip-flop stores the input information when the clock voltage becomes sufficiently positive to enable the input AND gate. The AND gate threshold voltage is given in Fig. 3 as a function of temperature. It is labeled $V_{AG\,th}$. Also given is the clock coupling transistor threshold voltage $V_{CP\,th}$. $V_{AG\,th}$ is an enabling voltage while $V_{CP\,th}$ is an inhibiting voltage. A rising clock voltage inhibits the clock coupling transistors at t_0 assuring that the "slave" flip-flop will not change. At t_1 the AND gates to the "master" flip-flop are enabled, storing the input information. A falling clock voltage disables the AND gates at t_2 preventing any further change in the "master" flip-flop. At t_3 the clock voltage falls below the inhibit level allowing the state of the "master" flip-flop to be transferred to the "slave" flip-flop.

2. Noise Immunity (Figs. 6-9)

   There are two types of noise immunity which might be guaranteed: Signal noise or Ground noise

   (A) Signal noise immunity

$$V_{NS} = \left| V_0(\max) - V_{0\,TH} \right|$$

or

$$V_{NS} = \left| V_1(\min) - V_{1\,TH} \right|$$

where

$V_{OH} = V_1(\min)$		Minimum High Output Voltage
$V_{OL} = V_0(\max)$		Maximum Low Output Voltage
$V_{IH} = V_{1\,TH}$		Minimum High Input Voltage That Guarantees Proper Operation

$V_{IL} = V_{0\,TH}$ Maximum Low Input Voltage That Guarantees Proper Operation

(B) Ground noise immunity, V_{NG}. The worst case noise immunity for the 931 element is ground noise V_{NG}. The worst case positive ground noise immunity circuit condition will occur when the clock input is at the lowest V_{CE}(sat) voltage. For the noise immunity Graphs No. 6, 7, 8, and 9, the minimum saturation voltage was assumed to be +50 mV.

Note that the curves show two values of noise immunity at a given temperature. The low value of V_{CC} corresponds to a worst case beta limitation in the 931 element. The uppermost value corresponds to a V_{CE} (sat) limitation in the "slave" flip-flop. In Graph No. 8 for fan-out = 6 at -55°C, the worst case V_{NG} noise immunity is +300 mV at $V_{CC} \approx$ +4.20 V. This corresponds to a worst case minimum signal noise immunity of >500 mV for the same fan-out, temperature, and power supply. Each of curves Fig. 6-9 shows V_n, the worst case of V_{NG} or V_{NS}.

Fig. 1
TYPICAL V_{OUT}-V_{CP} (CLOCK INPUT) TRANSFER CHARACTERISTIC

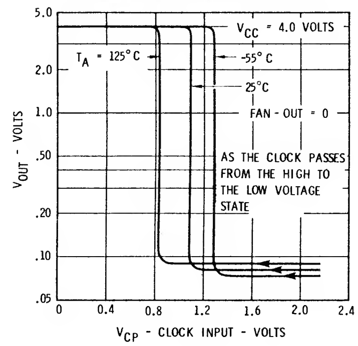


Fig. 2
TYPICAL V_{OUT}-V_{CP} (CLOCK INPUT) TRANSFER CHARACTERISTIC

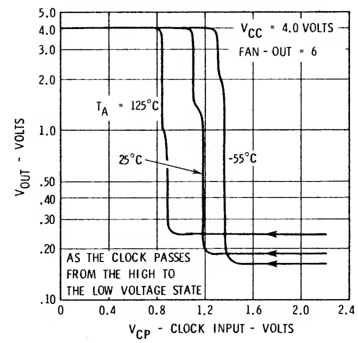


Fig. 3
TYPICAL THRESHOLD VOLTAGE VARIATION VERSUS TEMPERATURE FAN-OUT FROM n = 1 TO n = 9

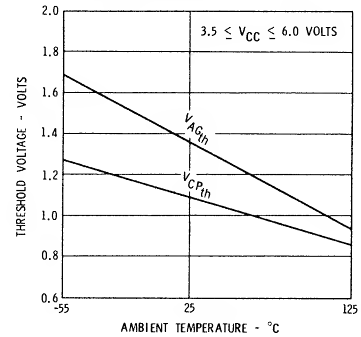


Fig. 4
OUTPUT SATURATION VOLTAGE VERSUS OUTPUT CURRENT TYPICAL

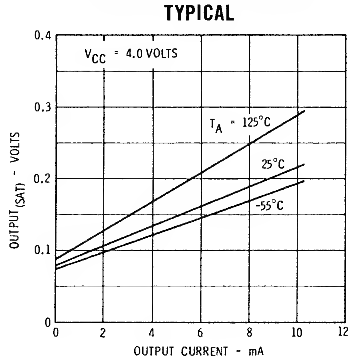


Fig. 5
POWER DISSIPATION VERSUS TEMPERATURE TYPICAL

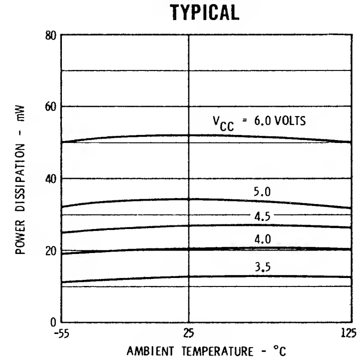


Fig. 6
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY

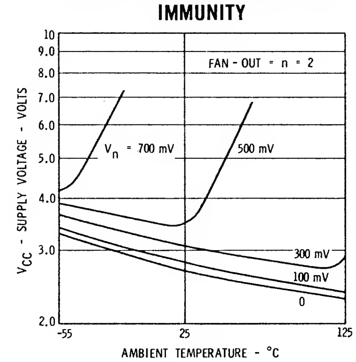


Fig. 7
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY

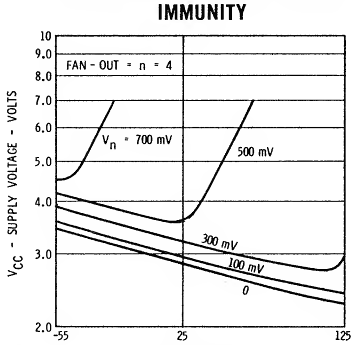


Fig. 8
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY

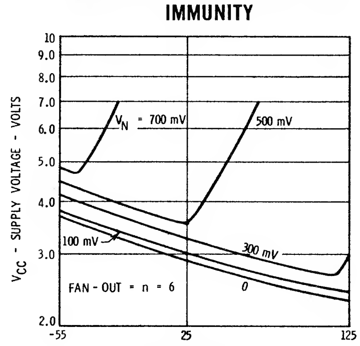
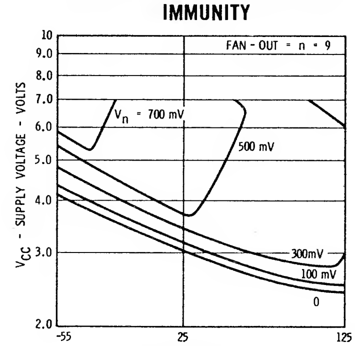
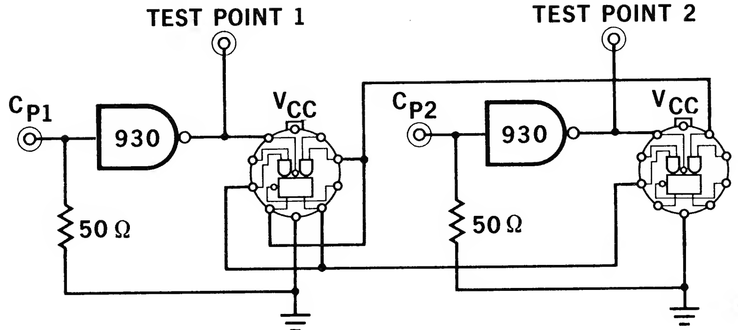
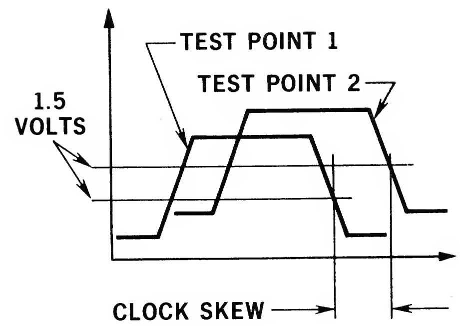


Fig. 9
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY



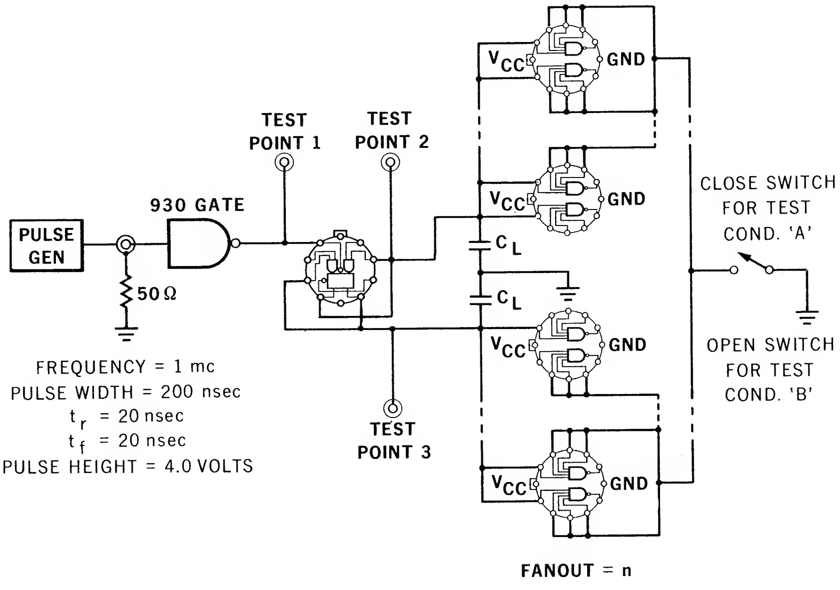
TEST CONDITIONS FOR FIGURE 10



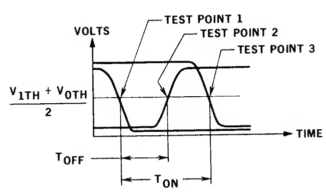


Clock skew is the maximum delay allowable between C_{P1} and C_{P2} which still results in reliably shifting information. Note that when C_{P2} occurs before C_{P1} there is <u>no</u> time delay restriction.

TEST CONDITIONS FOR FIGURES 11 THROUGH 27



FREQUENCY = 1 mc
PULSE WIDTH = 200 nsec
t_r = 20 nsec
t_f = 20 nsec
PULSE HEIGHT = 4.0 VOLTS



NOTES:

1. In test condition 'A' fan-out = n, n-1 inputs are inactive and only one is active.
2. In test condition 'B', n inputs are active.
3. Both outputs are equally loaded. Only loading on output going positive has major effect except at low V_{CC} and low temperature. Refer to DTμL Composite Data Sheet, pages 4 and 5.

Fig. 10
TYPICAL ALLOWABLE CLOCK SKEW VERSUS TEMPERATURE

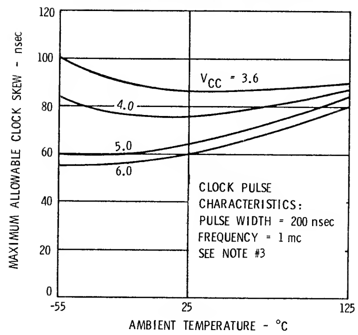


Fig. 11
MINIMUM CLOCK PULSE WIDTH REQUIRED TO SET AN 931 ELEMENT VERSUS TEMPERATURE — TYPICAL

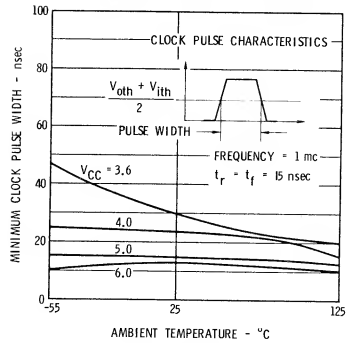


Fig. 12
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

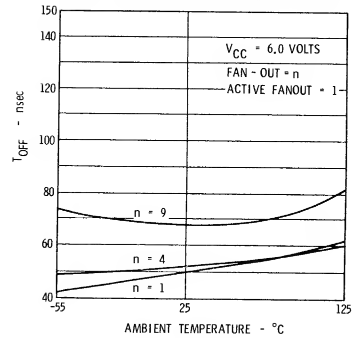


Fig. 13
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

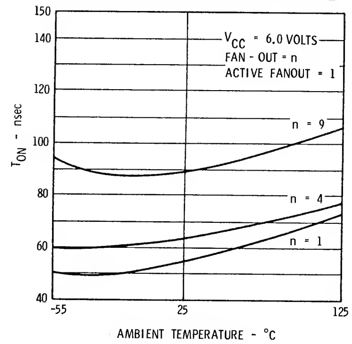


Fig. 14
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

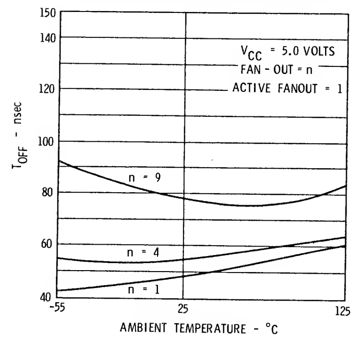


Fig. 15
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

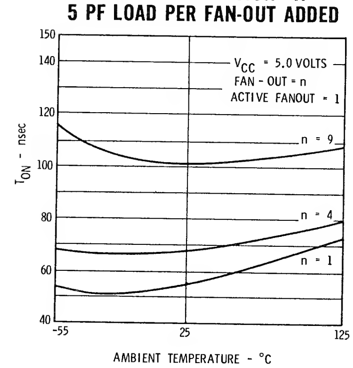


Fig. 16
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

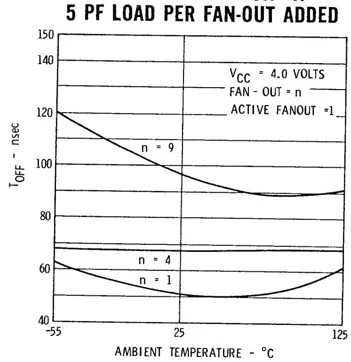


Fig. 17
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

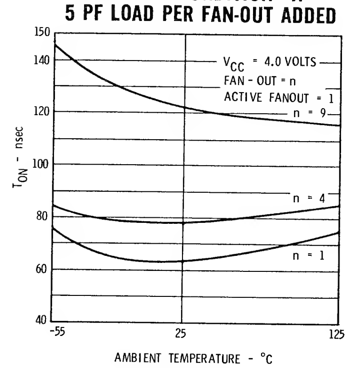


Fig. 18
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

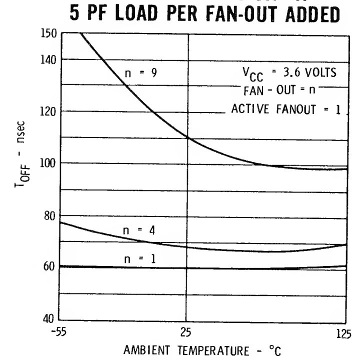


Fig. 19
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

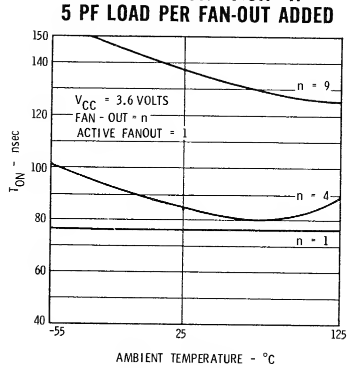


Fig. 20
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

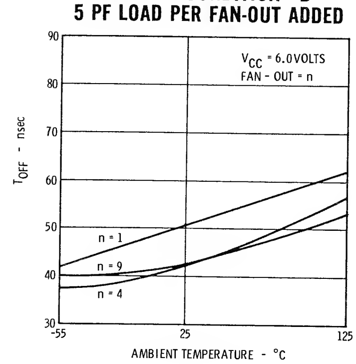


Fig. 21
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

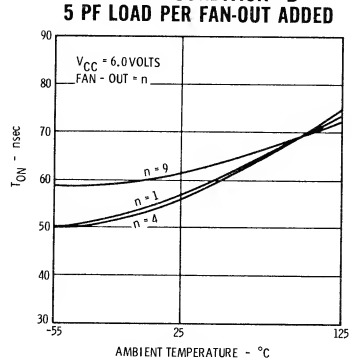


Fig. 22
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

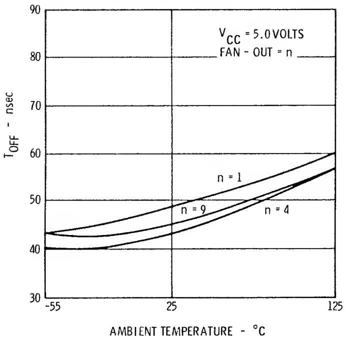


Fig. 23
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

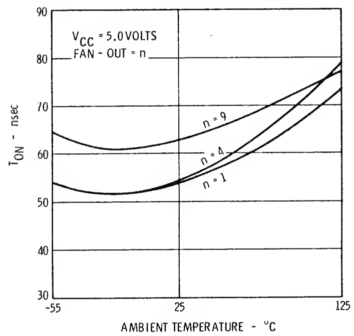


Fig. 24
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

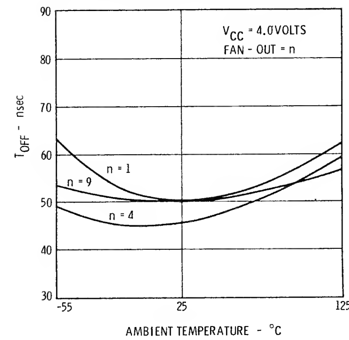


Fig. 25
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

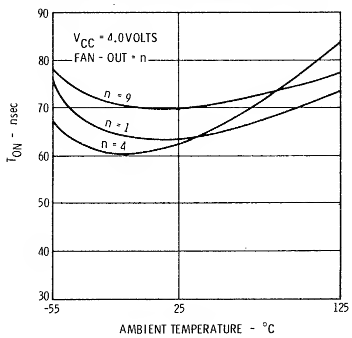


Fig. 26
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

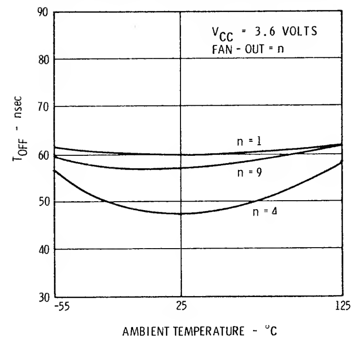
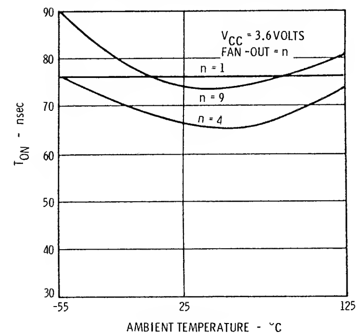
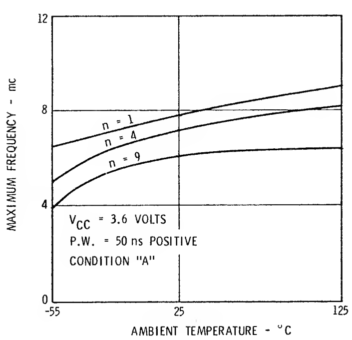
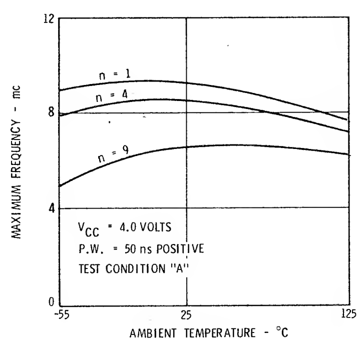


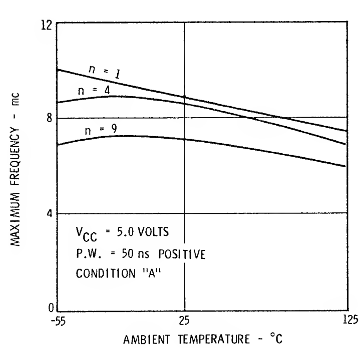
Fig. 27
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

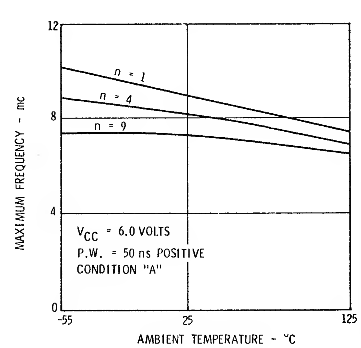


TYPICAL MAXIMUM FREQUENCY OF OPERATION VERSUS TEMPERATURE FOR A PULSE WIDTH OF 50nsec UNDER TEST CONDITION "A"
(5pf per fan-out)



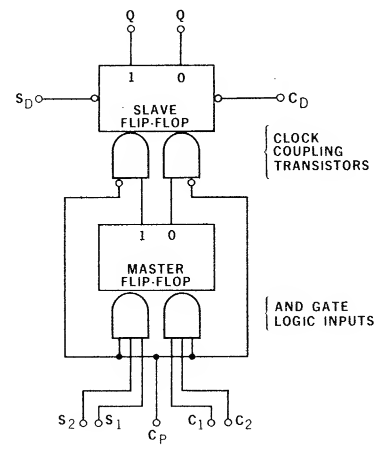




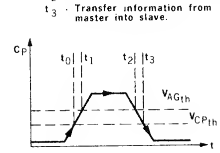


NOTE: Please refer to DTμL Composite Data Sheet, pages 4 and 5, for Capacitive loading effects and improvements with resistor shunting to V_{CC}.

FIG. A. EXPLANATION OF FIG. 3 $V_{AG_{th}}$ and $V_{CP_{th}}$.
(See note 1 for operation and terminology.)



CLOCK TIMING SEQUENCE
t_0 - Turn off clock coupling transistors.
t_1 - Enter logic into master FLIP-FLOP.
t_2 - Inhibit AND GATE input to master.
t_3 - Transfer information from master into slave.



APPLICATION DATA

The DTμL-931 Clocked Flip-Flop is a complete, self-sufficient, clocked storage element. It is directly coupled throughout and hence, does not depend on capacitors, propagation delays, or charge storage effects to achieve reliable time separation and retention of input logic values. As a direct consequence, its inputs are not sensitive to rise or fall times of logic signals, nor to pulse widths. It responds exclusively to input voltage levels with definite, separated thresholds for both the low and high input voltage levels.

Two types of data entry are possible: Synchronous, requiring the concurrence of an active voltage level at the trigger input as well as the associated synchronous input, and asynchronous, requiring nothing more than the active signal level at the appropriate asynchronous inputs.

Synchronous Entry

The entry of information at the synchronous inputs, set (S) and clear (C), is under direct control of the trigger (T) input. Input signals formed at the input AND gates are entered into the first of two simple latch circuits, hereafter referred to as "master" and "slave," when the trigger input is high, and thereafter transferred to the "slave" when the trigger input becomes low. The "slave" outputs are the outputs for the aggregate unit. The synchronous inputs are inhibited during the time interval when the outputs of Clocked Flip-Flops are changing, thus preventing more than one change in output for each cycle of the trigger input from low to high and back.

The state of the "master" just prior to the negative excursion of the trigger signal represents the condition which the "slave" outputs will assume. The constraints placed upon the synchronous inputs while the trigger level is high are: The inputs must be settled and stable for a sufficient time to permit the "master" to assume a definite condition, and the inputs must not be simultaneously active (high). To permit unrestricted use of the input AND gates, a necessary and sufficient condition for trouble-free operation is that synchronous logic inputs may change only while the trigger input signal is low.

Waveform Below

1. Synchronous logic inputs stable
2. Enter "master"
3. Transfer "master" to "slave"
4. Propagate through logic gates

Asynchronous Entry

Asynchronous Entry is made at the "slave." Therefore, it is clear that one cannot use the asynchronous inputs without regard for the synchronous inputs if well-defined operation is to result. The trigger input must be high during asynchronous entry so that the "master" outputs will not conflict with the asynchronous inputs.

The necessity for a high trigger input during asynchronous entry precludes use of the asynchronous inputs when the trigger signal for each stage is not under complete control except for certain specific conditions. For example, a ripple-carry counter, where the trigger input of each stage is connected to an output of the previous stage. Here, because, of the signal polarities involved, it is only possible to clear all "slaves" if the counter is a reverse counter or set all "slaves" if it is a forward counter. In neither case is it possible to set an arbitrary pattern reliably.

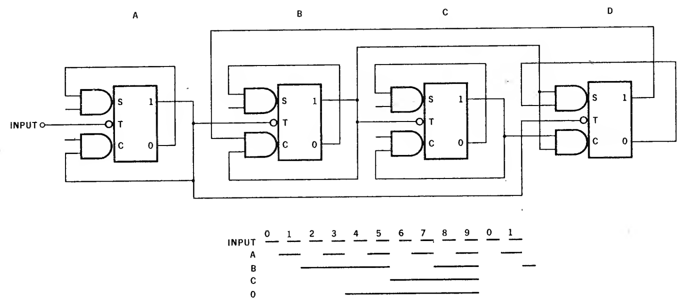
Arbitrary asynchronous entry to shift registers is straightforward because the shift signal (trigger input) may be held high at will. Due to the direct connection between the "slave" of one stage and the "master" of its successor, the information entered into the "slave" of one stage will automatically be transferred to the "master" of the next. Therefore, the next negative excursion of the shift pulse will result in shifting information one stage - the desired response. At the input stage to the shift register, where serial information originates, care must be exercised to insure that the initial "master" flip-flop is set to the proper condition, corresponding to the next bit of information that is to appear in this stage.

A general consideration in asynchronous entry is propagation time. After modifying the state of "slaves" asynchronously, adequate time must be allotted for signal propagation through all intervening logic networks before resuming synchronous operation. Furthermore, signal races due to different signal path lengths become a possibility.

Since asynchronous entry condones changing logic inputs during the time that trigger input signals are high - an otherwise forbidden situation in a synchronous system - particular care is required when both of the Clocked Flip-Flop AND gate inputs are used. A common case is J-K mode operation (stage outputs cross-connected to their own inputs). Here, one input AND gate is always inhibited; and, while the other input can cause the "master" flip-flop to change, the inhibited input cannot return the "master" to its initial state if the final input value does not indicate that a change of the overall state is required. Thus, when the clock input next goes low, transferring "master" to "slave," an erroneous output can ensue.

Similar remarks apply to more complex interconnections, and the designer should always assure himself that asynchronous entry does not create a conflict in some unsuspected way.

1-2-4-2 DECADE USING DTμL 931 CLOCKED FLIP-FLOPS

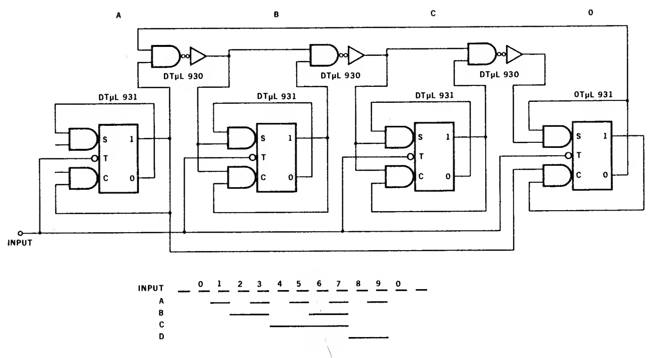


COUNT SEQUENCE

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1
0	0	0	0

etc.

SYNCHRONOUS SERIAL CARRY 1-2-4-8 DECADE

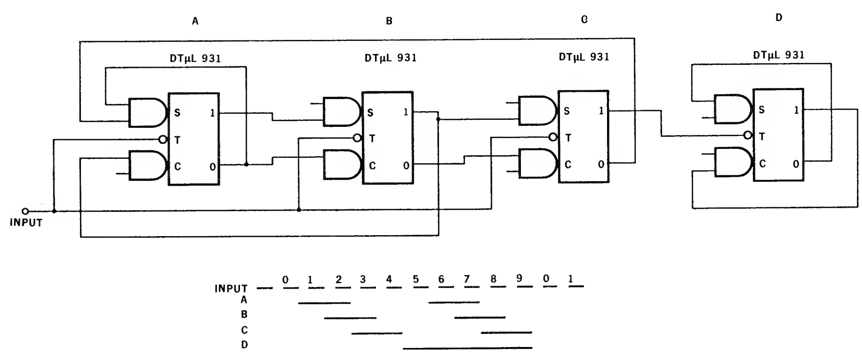


COUNT SEQUENCE

A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	0	0	0

etc.

CODED BIQUINARY DECADE COUNTER

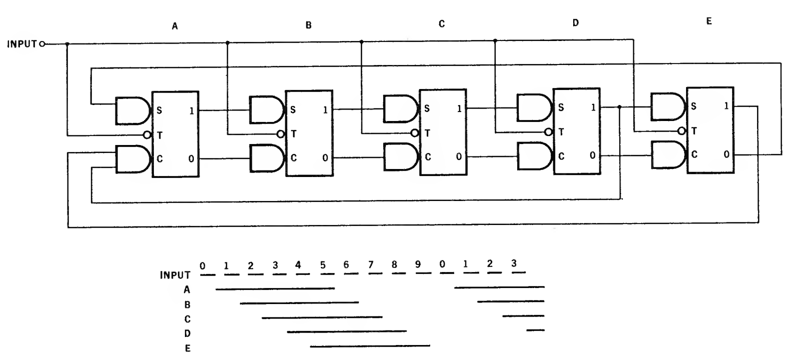


COUNT SEQUENCE

A	B	C	D
0	0	0	0
1	0	0	0
1	1	0	0
0	1	1	0
0	0	1	0
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	1
0	0	1	1
0	0	0	0

etc.

MODULO-10 SHIFT COUNTER USING DTμL931'S



COUNT SEQUENCE

A	B	C	D	E
0	0	0	0	0
1	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1
0	1	1	1	1
0	0	1	1	1
0	0	0	1	1
0	0	0	0	1
0	0	0	0	0

etc.

DTμL 932 DUAL BUFFER ELEMENT
DTμL 944 DUAL POWER GATE ELEMENT
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION - The DTμL 932 Dual Buffer Element and the DTμL 944 Dual Power Gate Element are dual 4-input inverting drivers for use with the Fairchild Diode-Transistor Micrologic Family or any similar DTL logic circuits. The fan-in of either element may be extended with the use of the DTμL 933 Element. Input thresholds and currents are the same as other DTμL gate elements.

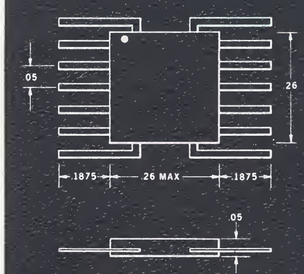
Both DTμL 932 and DTμL 944 Elements have typical saturation resistances of 5 ohms which allow output currents of up to 100 mA. The DTμL 932 features an emitter-follower output pull-up, which provides a high fan-out device with superior capacitance-driving capability.

The DTμL 944 features an output with no internal pull-up. Thus, 944 outputs may be tied together for the "wired-OR" function, or may drive inputs with logic thresholds of 4 to 6 volts. The 944 is intended as a high fan-out gate interface driver, or low-power lamp driver. An external pull-up resistor may return to the nominal DTμL V_{CC} supply of 5 volts or to other supplies up to 12 volts. These supplies may be located near the output or at the far end of an open transmission line or twisted pair interconnection.

Complete test specifications, typical and worst-case DC curves, t_{pd} curves, and suggested loading rules are included in these specifications.

TYPICAL FLAT PACKAGE

TOP VIEW

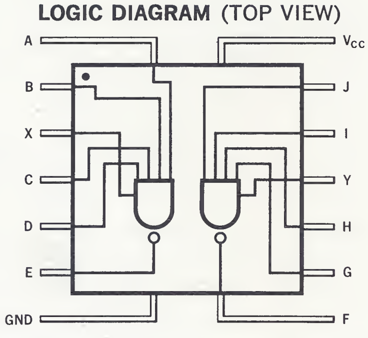


PART NO's
9X93251—932 ELEMENT
9X94451—944 ELEMENT
X = 3 CERPAK
X = 5 10 PIN TO-5

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}), -55°C to +125°C, Continuous	+8.0 Volts	Input Reverse Current	5.0 mA
Supply Voltage (V_{CC}), pulsed, < 1.0 sec.	+12 Volts	Operating Ambient Temperature	-55°C to +125°C
Output Current, into Outputs, Continuous	150 mA	Storage Temperature	-65°C to +150°C
Output Current, into Outputs, pulsed, <30 milliseconds	300 mA	Operating Junction Temperature (See note A on page 2)	+175°C Maximum
Input Forward Current	-10 mA		

LOGIC DIAGRAM (TOP VIEW)



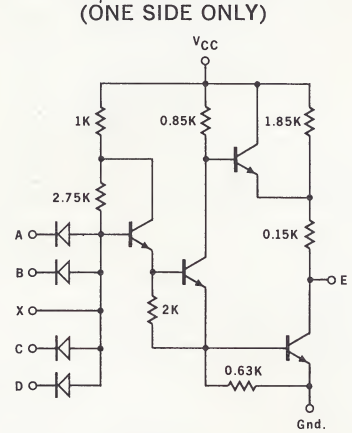
POSITIVE (NAND) LOGIC

$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$
$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

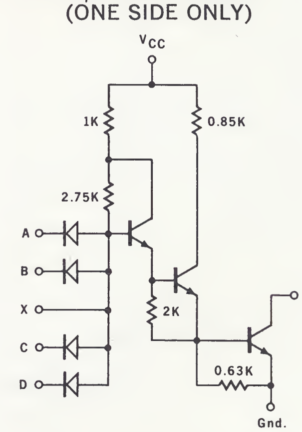
NEGATIVE (NOR) LOGIC
(symbol not shown)

$E = \overline{A+B+C+D+(X)}$
$F = \overline{G+H+I+J+(Y)}$

SCHEMATIC DIAGRAM OF THE DTμL 932 ELEMENT
(ONE SIDE ONLY)



SCHEMATIC DIAGRAM OF THE DTμL 944 ELEMENT
(ONE SIDE ONLY)



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING.

TEST SEQUENCE DTμL 932 AND DTμL 944 ELEMENTS

NOTE: Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	LTPD Group	Notes	Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	Limits Min.	Limits Max.
1, (2)	A		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	$V_E(V_F)$		V_{OL}
3, 4, 5, 6, (7, 8, 9, 10)	B	1, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
11, (12)	C		V_R	GND	GND	GND			V_{CCH}	$I_A(I_G)$		I_R
13, (14)	C		GND	V_R	GND	GND			V_{CCH}	$I_B(I_H)$		I_R
15, (16)	C		GND	GND	V_R	GND			V_{CCH}	$I_C(I_I)$		I_R
17, (18)	C		GND	GND	GND	V_R			V_{CCH}	$I_D(I_J)$		I_R
19, (20)	D		V_F	V_R	V_R	V_R			V_{CCH}	$I_A(I_G$		I_F
21, (22)	D		V_R	V_F	V_R	V_R			V_{CCH}	$I_B(I_H)$		I_F
23, (24)	D		V_R	V_R	V_F	V_R			V_{CCH}	$I_C(I_I)$		I_F
25, (26)	D		V_R	V_R	V_R	V_F			V_{CCH}	$I_D(I_J)$		I_F
27, (28)	C	3	GND					V_{CEX}	V_{CEX}	$I_E(I_F)$		I_{CEX}
29, (30)	B	2, 3	GND					GND	V_{CCH}	$I_E(I_F)$	I_{SC}	
31	E								V_{PD}	I_{VCC}		I_{PDH}
32	E	2	GND						$V_{(max)}$	I_{VCC}		$I_{(max)}$
33, (34)	E	3					V_X	I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
35, 36	F	t_{pd+}, t_{pd-} See Table of test circuit conditions and limits.										
35, 36, 37, 38 (39, 40, 41, 42)	B	1, 4	V_{IL}	V_{IL}	V_{IL}	V_{IL}		V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
43, (44)	B	4					V_X	V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
45, (46)	B	4	GND					I_{CE}	V_{CCH}	$V_E(V_F)$	LV_{CE}	

NOTES:

(1) V_{IL} applied individually to 1 input each test. Other inputs open.

(2) Apply GND to both pins A and G.

(3) DTμL 932 only.

(4) DTμL 944 only.

(5) On 10 Pin TO-5 units, pins D, X, I and J are omitted. Thus tests 6, 9, 10, 16, 17, 18, 24, 25, 26, 33, 38, 41, 42 and 43 do not apply.

TEST LIMITS—DTμL 932 AND DTμL 944

	Units	-55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max
V_{OL}	Volts		0.4		0.4		0.45
V_{OH}	Volts	2.6		2.5		2.5	
I_R	μA		2.0		2.0		5.0
1 I_F	mA		-1.6		-1.6		-1.5
I_{CEX}932	μA		50				
I_{SC}(min)932	mA	-16		-18		-16	
$I_{(max)}$932&944	mA				6.0		
I_{PDH}944	mA				20		
I_{PDH}932	mA				26.6		
I_{CEX}944	mA		0.05		0.1		0.2
LV_{CE}944	Volts				6.0		

CONDITIONS AND LIMITS, t_{pd} TESTS

(V_{CC} = 5.0 V, T_A = 25°C)

		R	C	Min.	Max.	
t_{pd+}	944	510 Ω	20 pf	15 nsec	50 nsec	
t_{pd-}	944	150 Ω	100 pf	10 nsec	35 nsec	
t_{pd+}	932	510 Ω	500 pf	25 nsec	80 nsec	
t_{pd-}	932	150 Ω	500 pf	15 nsec	40 nsec	
t_{pd+}	944	150 Ω	20 pf	10 nsec	35 nsec	(Note 1)
t_{pd-}	944	510 Ω	20 pf	5.0 nsec	20 nsec	(Note 1)
t_{pd+}	932	150 Ω	500 pf	20 nsec	65 nsec	(Note 1)
t_{pd-}	932	510 Ω	200 pf	8.0 nsec	30 nsec	(Note 1)

NOTE: Correlating limit provided as design information only.

FORCING CONDITIONS

	Units	-55°C	+25°C	+125°C
$V_{(max)}$	Volts	--	8.0	--
V_{PD}	Volts	--	5.0	--
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_R	Volts	4.0	4.0	4.0
V_F	Volts	0	0	0
V_{CEX}	Volts	4.5	4.5	4.5

	Units	-55°C	+25°C	+125°C
I_{OL}944	mA	36	40	36
I_{OL}932	mA	34	36	32
I_{OH}932	mA	-2.0	-2.5	-4.0
V_{IL}	Volts	1.4	1.1	0.8
V_{IH}	Volts	2.1	1.9	1.7
V_X	Volts		1.8	
I_{CE}944	mA		5.0	

NOTE A:

Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for cerpak. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for cerpak. Heat removal in cerpak is highly dependent upon contact surfaces or air flow and on lead attachment and Thermal paths thru leads, as well as number of soldered leads.

MINIMUM/MAXIMUM AND TYPICAL DC CURVES

FIG. 1. $-1\ I_F$ DTμL932, 944 MAXIMUM VS. TYPICAL

($T_A = -55°C$ & $+25°C$)

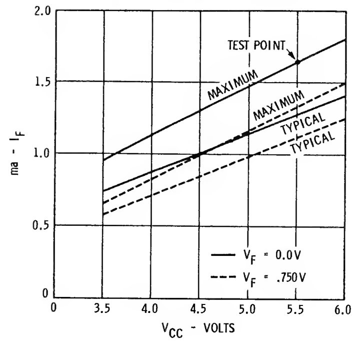


FIG. 2. DTμL INPUT THRESHOLDS VS. TEMPERATURE (932, 944)

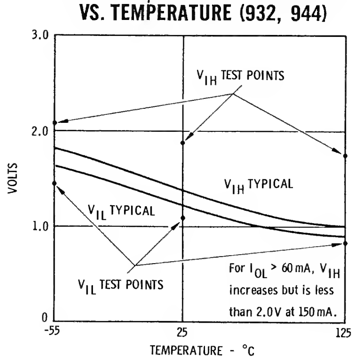


FIG. 3. TYPICAL POWER DISSIPATION PER SIDE VS. SUPPLY VOLTAGE (OUTPUT NOT LOADED) (932, 944)

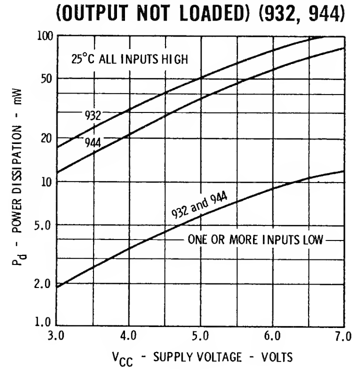


FIG. 4. TYPICAL OUTPUT CURRENT WITH INPUTS LOW (932)

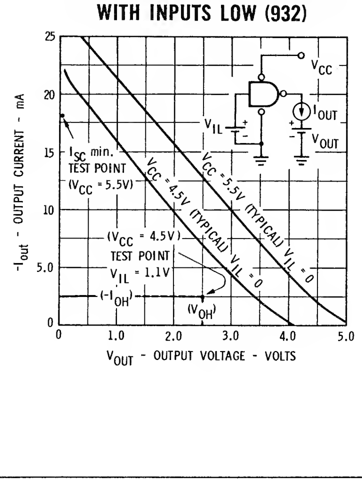


FIG. 5. TYPICAL OUTPUT LOW CURRENT VS. SUPPLY VOLTAGE ($-55°C$ and $+25°C$) (932)

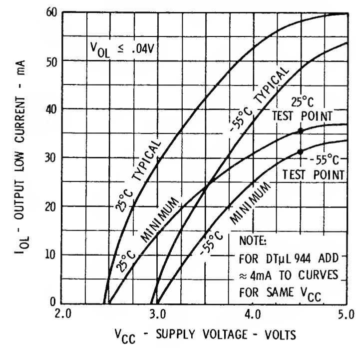


FIG. 6. TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (932)

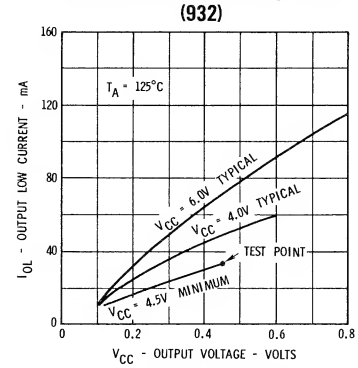
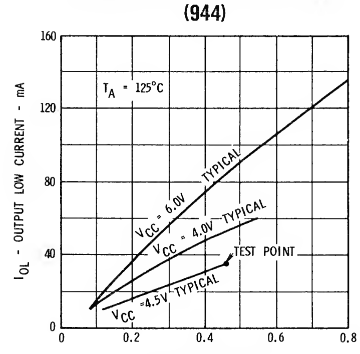


FIG. 7. TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (944)



t_{pd} CURVES

FIG. 8. TYPICAL $t_{pd}-$ VS. CAPACITY (932, 944)

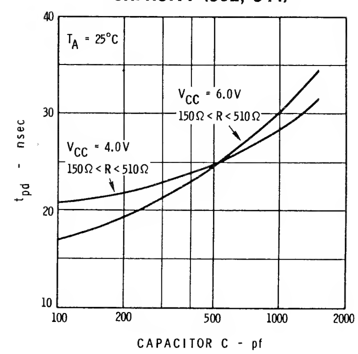


FIG. 9. TYPICAL $t_{pd}+$ VS. CAPACITY (944)

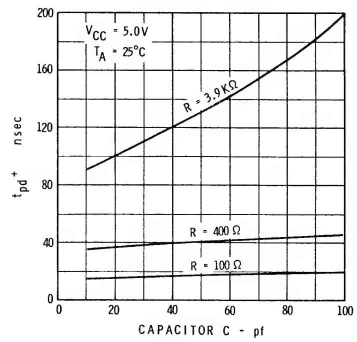
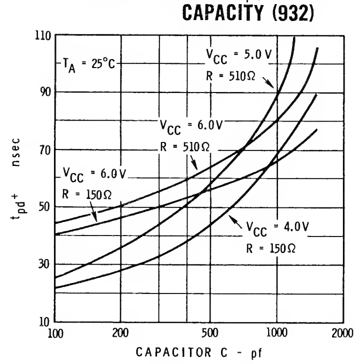
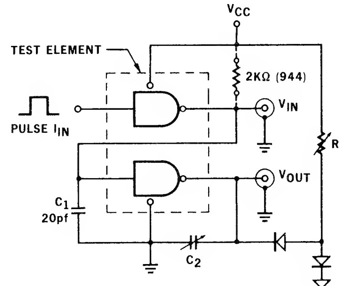
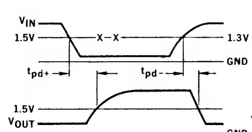


FIG. 10. TYPICAL $t_{pd}+$ VS. CAPACITY (932)



t_{pd} TEST CIRCUIT FOR DTμL 932 ELEMENT



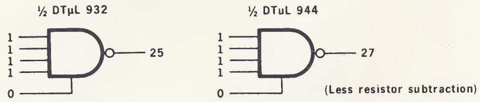


All Diodes are FD600 or Equivalent at 25°C

C_1 and C_2 includes Probe and Jig Capacitance

NOTE:
The same circuit is used on the DTμL 944 element except that all diodes are omitted. The resistor R is tied to capacitor C and the Test Output. A 2KΩ resistor is used to load the input gate.

SUGGESTED INPUT-OUTPUT LOADING FACTORS (Please refer to DTµL Composite Data Sheet for complete family rules).



INPUT LOAD FACTORS FOR OTHER DTµL ELEMENTS

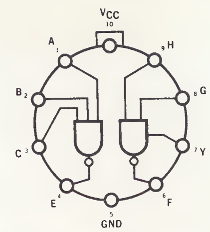
1 - DTµL 930, 946, 932, 944 inputs
2 - DTµL 931, 945, 948 CP pin
2/3 - DTµL 931, 945, 948 S_1 S_2 C_1 C_2
3/4 - DTµL 931 S_D C_D pins
2 - DTµL 945, 948 S_D C_D pins
1 - TTµL 103, 104 when driven by DTµL 932 or 944 with external resistor $\leq 510\,\Omega$.

MISCELLANEOUS RULES

1. DTµL 932 may not be output "OR"ed.
2. For increased current, inputs and outputs of 1/2 DTµL 932 or 1/2 DTµL 944 may be paralleled up to 4 common outputs. Each combined input = 4 loads. Combined output = 100 loads.
3. DTµL 944 may be output "OR"ed.
4. An external resistor should be used with DTµL 944. With external R to 5 volt V_{CC} ± 0.5 V; subtract output loads as follows:

   R = 2 KΩ - 2 loads
   R = 1 KΩ - 4 loads
   R = 510 Ω - 8 loads

10 LEAD TO-5 PACKAGE

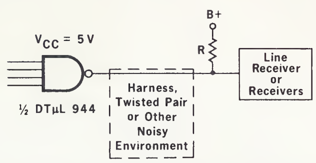


DTµL 930 DUAL GATE
DTµL 932 DUAL BUFFER
DTµL 944 DUAL POWER GATE

MISCELLANEOUS APPLICATIONS

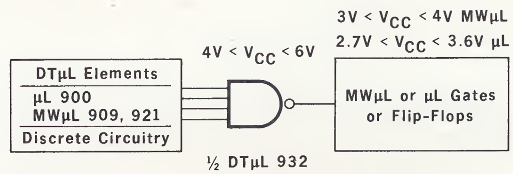
NOTE: In some of these applications, use of the elements is made within the design of the element but beyond the guaranteed test limits on page 2. Consult your Fairchild sales representative for additional information and/or selection requirements.

INTERFACING



B^+ up to 12 volts. Line Receiver may have nominal low level ≤ 1 volt; nominal threshold ≈ 4 V and nominal high level ≥ 8 V, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system. For a guaranteed V_{OH} level above 6 volts, an LV_{CE} selection may be desirable; for use of resistor that requires the 944 to sink more than 40 mA (at V_{OL} above .40 volt), a high current I_{OL} - V_{OL} selection may be desirable.

DRIVING µL AND MWµL

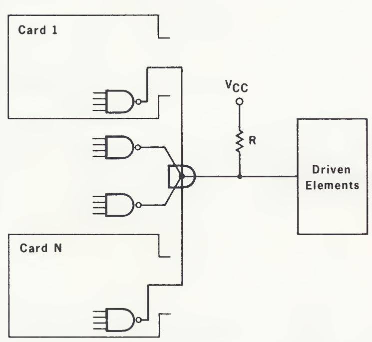


Rules: With V_{CC} > 4.5 V a 932 will drive 25-unit µLogic loads or 100 MWµL unit loads.

Derate DTµL output drive by 25% for DTµL 932 V_{CC} = 4 V.

Refer to DTµL 932 Output Current vs Output Voltage curve, Page 3, for matching to µL-MWµL $I_{AVAILABLE}$ requirements.

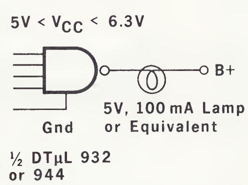
POWER GATING



Each output driver is 1/2 DTµL 944. Note that the DTµL 944 is a direct high fan-out replacement for DTµL 930, except that an external resistor must be used.

LAMP DRIVING

Suggested Ratings $T_A \leq 75°C$
Power Dissipation TO-5 400 mW Maximum
Power Dissipation Cerpak 240 mW Maximum



Maximum "hot" lamp current	
120 mA TO-5	one side only ON
100 mA Cerpak	one side only ON
90 mA TO-5	both sides ON
75 mA Cerpak	both sides ON

"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA.

The most significant thermal time constants for 932 and 944:

TO-5 Package	50 msec	Cerpak	100 msec

Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate. A high current β selection is desirable in this application.

DTμL 950 PULSE TRIGGERED BINARY

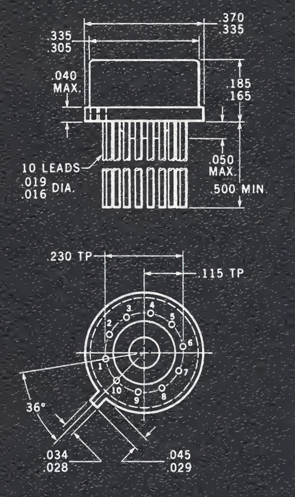
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION - The Fairchild Diode-Transistor Micrologic Pulse-triggered Binary is a high-speed gated flip-flop which may be used in any application requiring an R-S Flip-Flop or Counter Stage. It will operate as a binary counter in excess of 20 Mc over the full military temperature range of -55°C to +125°C, and typically dissipates less than 30 milliwatts of power.

The Pulse-triggered set and clear inputs are capacitively-coupled, but may be individually inhibited through their corresponding directly-coupled steering inputs. The pulse-triggering networks may be bypassed entirely through the use of the direct set and clear inputs, which respond to DC levels.

The DTμL 950 is ideally suited for preset ripple-carry counters and similar pulse-triggered applications. Some applications of the DTμL 950 are given on Page 2.

PHYSICAL DIMENSIONS
(SIMILAR TO TO-5)

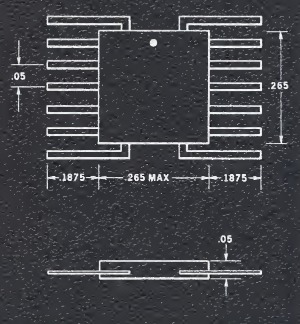


NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

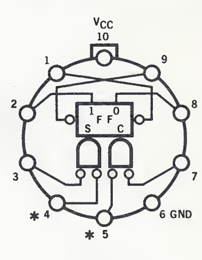
Supply Voltage (V_{CC}), -55°C to +125°C Continuous	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1.0 sec.	+12 Volts
Output Current, into Outputs, Continuous	50 mA
Output Current, into Outputs, pulsed, <30 milliseconds	100 mA
Input Forward Current, Pins 1, 4, 10, 13	-10 mA
Input Reverse Current	5.0 mA
Input Voltage, Pins 5, 6	-1.0 Volt or +8.0 Volts
Operating Ambient Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Operating Junction Temperature (See Note A, Page 2)	+175°C Maximum

PHYSICAL DIMENSIONS
TYPICAL FLAT PACKAGE
TOP VIEW



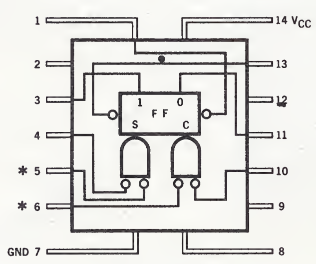
LOGIC DIAGRAM

TYPICAL TO-5 PACKAGE



Top View

TYPICAL FLAT PACKAGE



Top View

* These inputs are capacitively coupled.

PACKAGE CONVERSION

TO-5 Pin Number	FLAT PACKAGE Pin Number
1	1
2	3
3	4
4	5
5	6
6	7
7	10
8	11
9	13
10	14

PURCHASING INFORMATION
PAGE 4

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SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING.

TRUTH TABLES

RESPONSE TO

PULSE INPUTS						DIRECT INPUTS			
INPUTS				OUTPUTS		INPUTS		OUTPUTS	
4	5	6	10	3	11	1	13	3	11
H	X	H	X	NC	NC	H	H	NC	NC
X	H	X	H	NC	NC	L	H	L	H
L	L	X	H	H	L	H	L	H	L
L	L	H	X	H	L	L	L	H	H
H	X	L	L	L	H				
X	H	L	L	L	H				
L	L	L	L	AMBIGUOUS					

NOTES:

(1) Pin numbers refer to flat package.

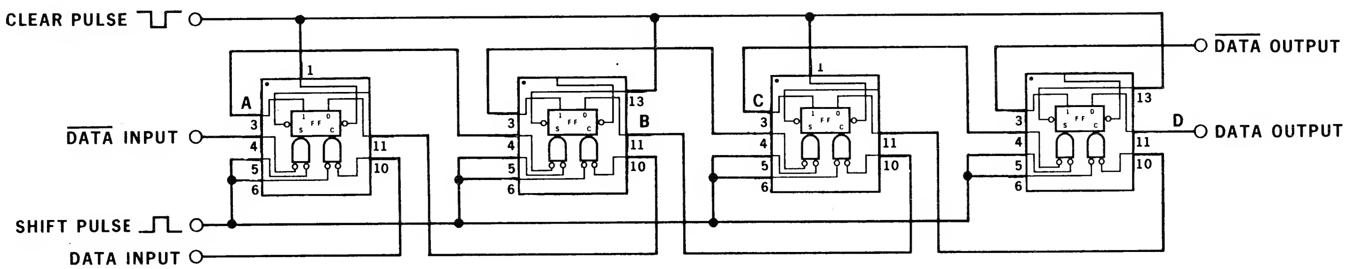
(2) Abbreviations used in the body of tables:

- L = low, the more negative voltage level
- H = high, the more positive voltage level (In all cases, unused pins have the same effect as high.)
- X = immaterial, either H or L has equal effect.
- NC = no change, the trigger-pulse has no effect on outputs.

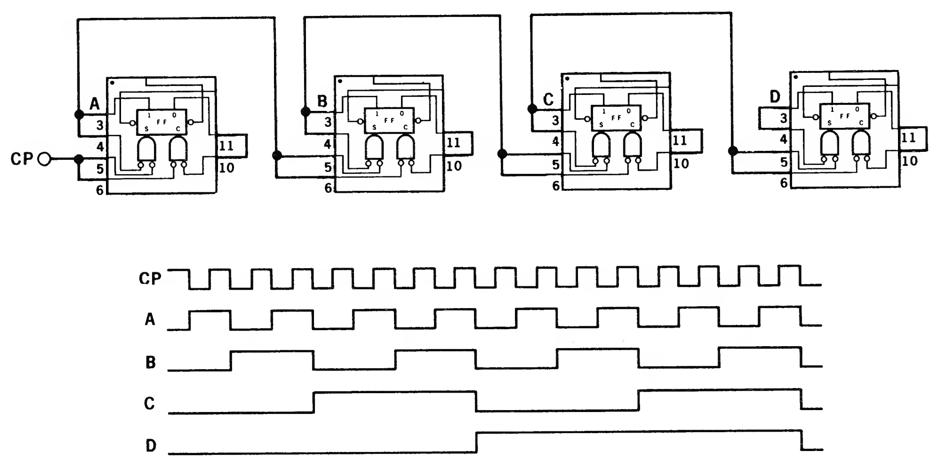
(3) H or L for pins 5 and 6 represent voltage transitions to the level indicated rather than the levels themselves.

(4) The tables assume independent use of pulsed inputs and direct inputs. Otherwise, direct inputs will predominate.

SHIFT REGISTER



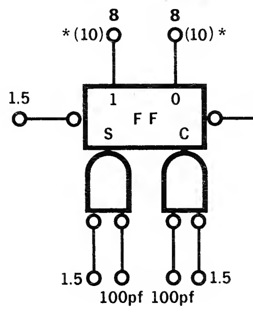
RIPPLE-CARRY BINARY COUNTER



NOTE A:

Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for cerpak. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for cerpak. Heat removal in cerpak is highly dependent upon contact surfaces or air flow and on lead attachment and Thermal paths through leads, as well as number of soldered leads.

SUGGESTED INPUT-OUTPUT LOADING FACTORS



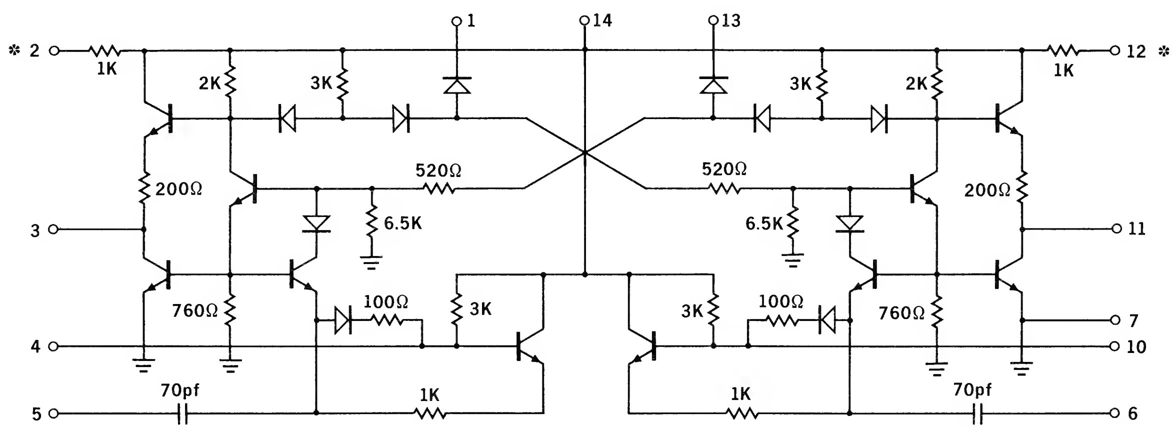
*(0°C to + 75°C)

INPUT LOAD FACTORS FOR OTHER DTμL ELEMENTS

1	-	DTμL 930, 946, 932, 962 inputs
2	-	DTμL 931, 945, 948 CP pin
2/3	-	DTμL 931, 945, 948 S_1 S_2 C_1 C_2
3/4	-	DTμL 931 S_D C_D pins
2	-	DTμL 945, 948 S_D C_D pins
1	-	TTμL 103, 104 when driven by DTμL 950

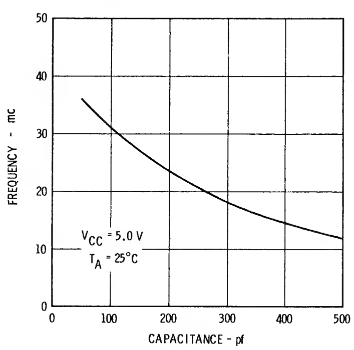
(Please refer to DTμL Composite Data Sheet for complete family rules.)

SCHEMATIC DIAGRAM OF DTμL 950

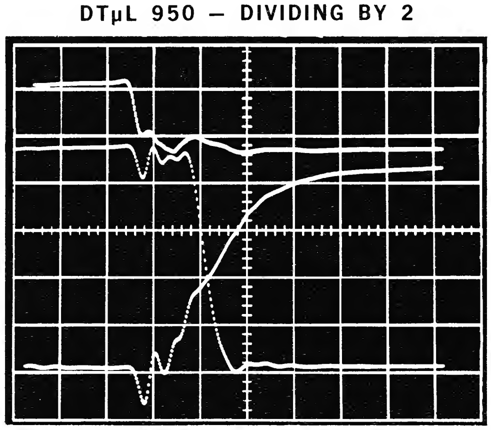


NOTE: Pin numbers refer to flat package.
* Unconnected on TO-5 package.

TYPICAL FREQUENCY OF OPERATION VS. LOADING CAPACITANCE



DTμL 950 — DIVIDING BY 2



10 nsec/division
25°C V_{CC} = 5.0 V

UPPER TRACE - Input to CP (2 volts/division)
POSITIVE GOING TRACE - Output Going High (1 volt/division)
NEGATIVE GOING TRACE - Output Going Low (1 volt/division)
20pf each output.

PURCHASING INFORMATION

To order part, the following part numbers should be used to expedite handling.

Ordering Part Number	Specific Element	Package
UX5995051X (−55 to 125° C)	DTμL 950	Low Profile TO-5
UX5995059X (0 to 70° C)	DTμL 950	Low Profile TO-5
UX3995051X (−55 to 125° C)	DTμL 950	¼ X ¼ Corning Cerpak
UX3995059X (0 to 70° C)	DTμL 950	¼ X ¼ Corning Cerpak

DTμL 945 • DTμL 948

CLOCKED FLIP-FLOP

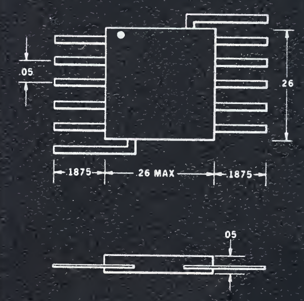
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION - The DTμL 945 and DTμL 948 Clocked Flip-Flops are directly-coupled units operating on the "master-slave" principle. Information enters the "master" while the Trigger input voltage is high and transfers to the "slave" when the Trigger input voltage goes low. Since operation depends only on voltage levels, any sort of waveshape having the proper voltage levels may be used as a trigger signal. Rise and fall times are irrelevant.

The DTμL 945 and DTμL 948 have an improved direct Set and Clear design which allows unhampered asynchronous entry irrespective of signals applied to any other inputs. The direct inputs always take precedence, thus simplifying the design of arbitrarily preset ripple-counters and other minimum hardware applications.

Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise. The DTμL 945 incorporates the standard 6 K-ohm output pull-up resistor, while the DTμL 948 features a 2 K-ohm output pull-up resistor for improved rise times, and matched delay between rising and falling outputs for capacitive loading up to 100 pf. Both the 945 and 948 provide increased fan-out capability and are pin-for-pin substitutes for the DTμL 931.

FLAT PACKAGE
(TOP VIEW)



NOTES:
All dimensions in inches

SYNCHRONOUS ENTRY

Inputs t_n 3	4	11	12	Output t_{n+1} 6
L	X	L	X	NC
L	X	X	0	NC
X	L	L	X	NC
X	L	X	L	NC
L	X	H	H	L
X	L	H	H	L
H	H	L	X	H
H	H	X	L	H
H	H	H	H	Undetermined

For J-K Mode Operation:
Connect 4 to 9 and 11 to 6

ASYNCHRONOUS ENTRY

Inputs 5	10	Outputs 6	9
H	H	NC	NC
H	L	H	L
L	H	L	H
L	L	H	H

*Asynchronous entry is independent of all other inputs and overrides synchronous entry.

SUGGESTED LOADING RULES (4.5V < V_{CC} < 5.5V)

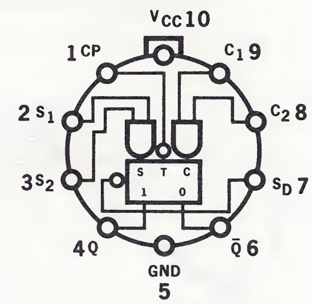
OUTPUT DRIVE

DTμL 945	10 (-55°C to +125°C)
DTμL 948	9 (-55°C to +125°C)
DTμL 945	12 (0°C to +75°C)
DTμL 948	11 (0°C to +75°C)

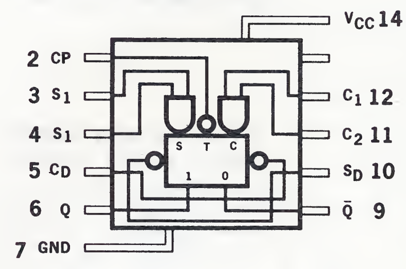
INPUT LOAD FACTORS

S_1, S_2, C_1, C_2 945, 948, 931	2/3
CP 945, 948, 931	2
S_D, C_D 945, 948	2
DTμL 930, 946, 962, 932, 944	1

TO-5
(TOP VIEW)



FLAT PACKAGE
(TOP VIEW)



NOTES:
(1) Pin numbers refer to flat package.
(2) Abbreviations used in the body of tables:
L = low, the more negative voltage level
H = high, the more positive voltage level
(In all cases, unused pins have the same effect as high.)
X = immaterial, either H or L has equal effect.
NC = no change, the trigger-pulse has no effect on outputs.

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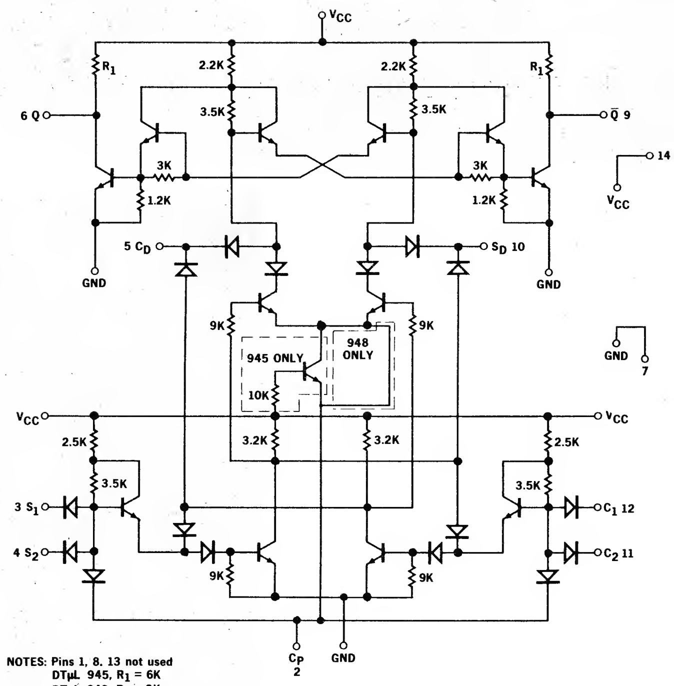
SCHEMATIC DIAGRAM



NOTES: Pins 1, 8, 13 not used
DTμL 945, R_1 = 6K
DTμL 948, R_1 = 2K

PIN NUMBERS REFER TO FLAT PACKAGE

PURCHASING INFORMATION:

Part Numbers:

-55°C TO 125°C

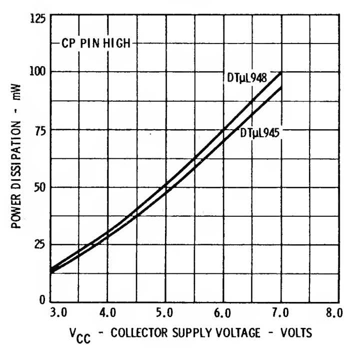
UX3994551X = CERPAK DTμL 945
UX3994851X = CERPAK DTμL 948
UX5994551X = 10 PIN TO-5 DTμL 945
UX5994851X = 10 PIN TO-5 DTμL 948

0°C TO 75°C

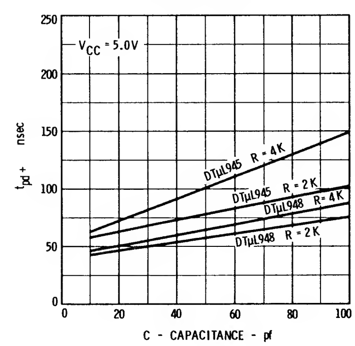
UX3994559X = CERPAK DTμL 945
UX3994859X = CERPAK DTμL 948
UX5994559X = 10 PIN TO-5 DTμL 945
UX5994859X = 10 PIN TO-5 DTμL 948

ELECTRICAL CHARACTERISTICS

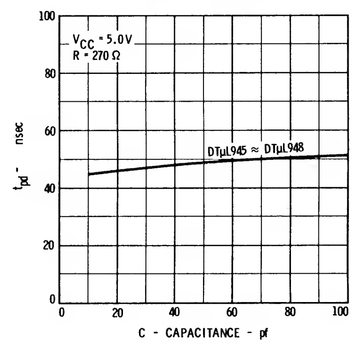
TYPICAL POWER DISSIPATION VS. V_{CC}



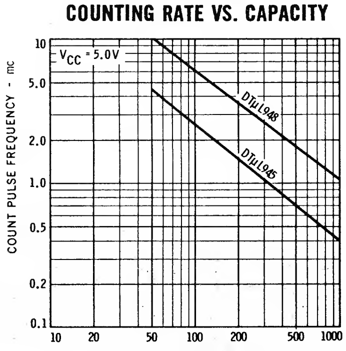
TYPICAL Tpd VS. CAPACITANCE *



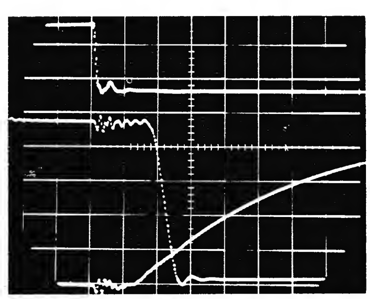
TYPICAL Tpd VS. CAPACITANCE *



TYPICAL MAXIMUM BINARY COUNTING RATE VS. CAPACITY



TYPICAL 948 DIVIDE BY TWO WAVEFORM



DTμL 948 as a binary counter
Upper Trace: Input, 2 volts per division
Lower Traces: Outputs, 1 volt per division
Falling output loaded by 50 pf and 330 Ω to V_{CC}.
Rising output loaded by 50 pf
25 nsec per division
V_{CC} = 5 V

* Refer to DTμL Composite data sheet for DTμL 931 switching time circuit

DTμL933 DUAL FOUR-INPUT EXTENDER ELEMENT

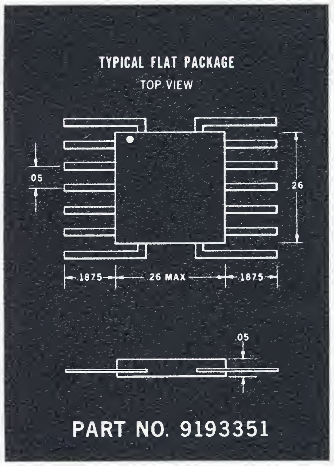
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

The DTμL 933 is a Dual Input-Extender consisting of two independent diode arrays identical in every respect to the input diodes of the DTμL Gate and Buffer elements. DTμL 933 elements may be used to extend fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the element to which they are connected.

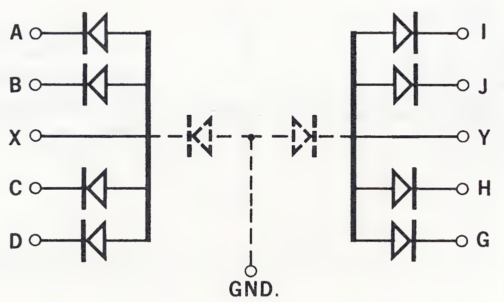
Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The effects of capacitance are summarized on the back page.

Typical input capacitance of DTμL 933 is 2 pf and output capacitance is 5 pf.

For complete test sequence and test values, please refer to the composite DTμL specification

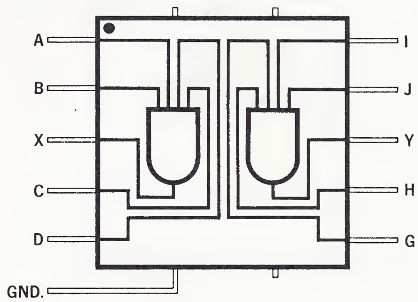


SCHEMATIC DIAGRAM

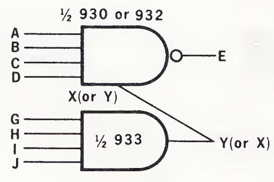


FLAT PACKAGE LAYOUT

(TOP VIEW)



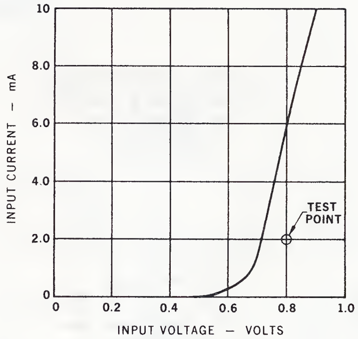
LOGIC EXAMPLE



POSITIVE LOGIC $E = \overline{A\ B\ C\ D\ G\ H\ I\ J}$

NEGATIVE LOGIC $E = \overline{A + B + C + D + G + H + I + J}$

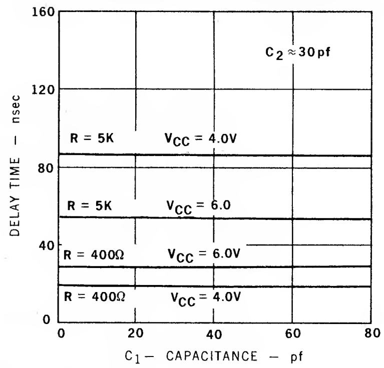
FORWARD VOLTAGE VS. FORWARD CURRENT + 25°C



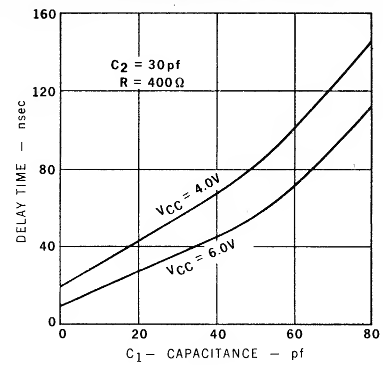
Typical Curves to Show the Effects of Extender Pin Capacitance (Resulting From the Use of DTμL 933) on Time Delay of DTμL 930 Dual Gate and DTμL 932 Dual Buffer

+ 25°C

DTμL 930 tpd + VS. EXTENDER PIN CAPACITANCE

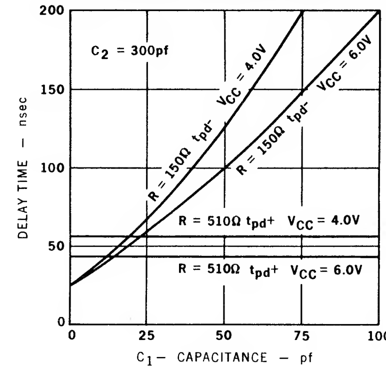


DTμL 930 tpd — VS. EXTENDER PIN CAPACITANCE



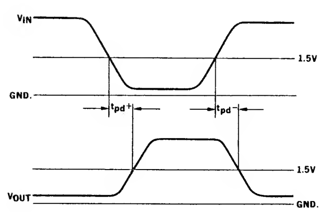
t_{pd}- at R = 5 KΩ is slightly lower.

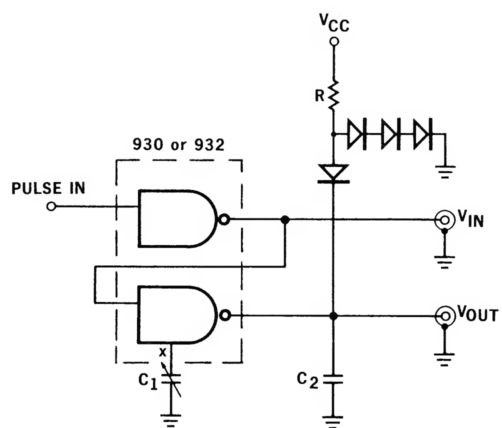
DTμL 932 TIME DELAY VS. EXTENDER PIN CAPACITANCE



TEST CONDITIONS

WAVESHAPES





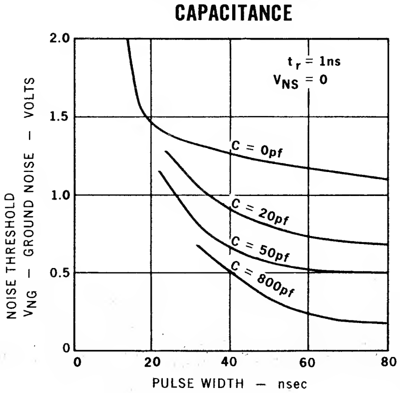
Diodes are FD600

C_1 represents the summation of the DTμL 933Dual Extender Element output capacitances (~5 pf per output) and associated board, connector and wiring capacitances.

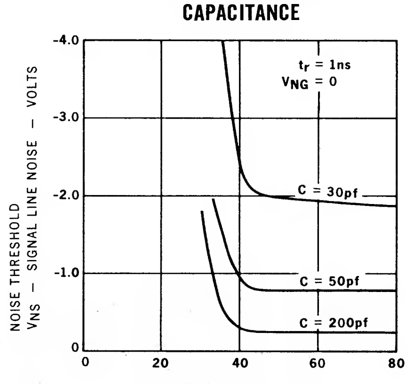
Typical Curves to Show the Effects of Extender Pin Capacitance on Noise Threshold of DTμL 930 Dual Gate

+ 25°C

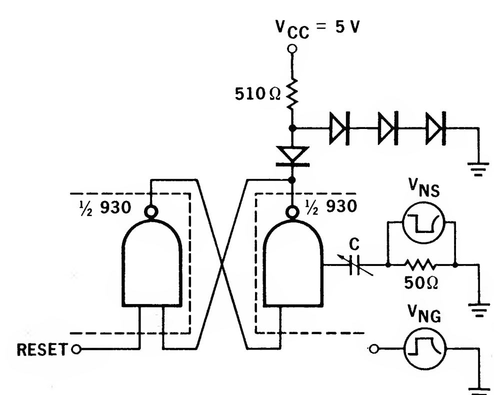
PULSED GROUND NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE



PULSED SIGNAL LINE NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE



TEST CONDITIONS



Diodes are FD600

DTμL 951

MONOSTABLE MULTIVIBRATOR

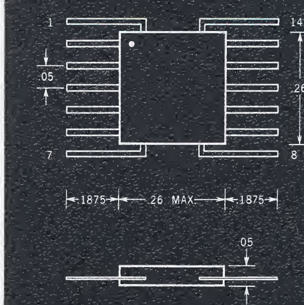
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION – The DTμL 951 Monostable Multivibrator is a monolithic silicon epitaxial integrated circuit for use with the Fairchild Diode-Transistor Micrologic Family or any other similar DTL logic elements. It provides complementary output pulses which are typically 100 nsec wide. This pulse width is adjustable by the addition of external discrete passive components.

The 951 element is compatible with the Fairchild DTμL Family over the full military temperature range of -55°C to +125°C and with a V_{CC} supply of 4.0 volts to 6.0 volts. The 951 element can also drive and be driven by Fairchild MWμL and μL elements.

The output pulse width is very stable as either V_{CC} or temperature (or both) is varied when an external timing resistor is used instead of the internal diffused resistor.

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACK)

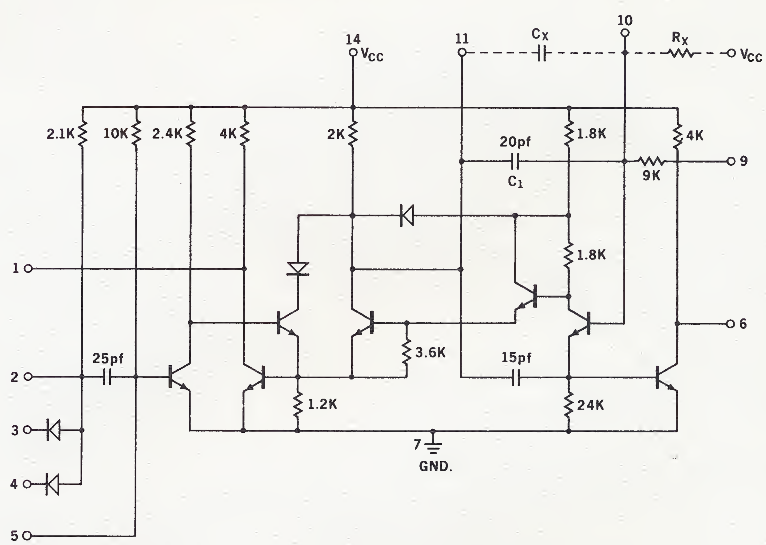


PART NO.
UX3995151X = CERPACK
UX5995151X = 10 PIN TO-5

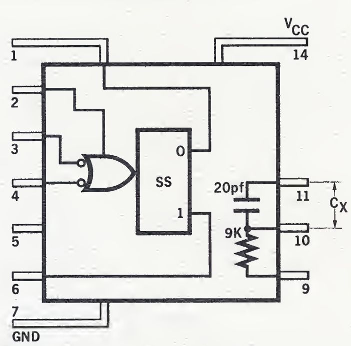
ABSOLUTE MAXIMUM RATINGS
(above which useful life may be impaired)

Supply Voltage (V_{CC}) -55°C to +125°C, continuous:	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1 sec.:	+12 Volts
Output Current, into outputs	50 mA
Current into Pin 10	5.0 mA
Input Forward Current	-10 mA
Input Reverse Current	1.0 mA
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM (Top View)



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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING.

TEST SEQUENCE

FORCING FUNCTIONS

Test No.	CERPAK Pin no.: / TO-5 Pin no.:	5 / –	1 / 7	2 / 8	3 / 9	4 / -	6 / 10	7 / 1	9 / 2	10 / 3	11 / 4	14 / 6	Note 1 Sense	Limits Min.	Limits Max.
1				V_F				GND				V_{CCH}	I_2	$.5 I_F$	
2					V_F	V_R		GND				V_{CCH}	I_3	$.5 I_F$	$2 I_F$
3	Note 2				V_R	V_F		GND				V_{CCH}	I_4	$.5 I_F$	$2 I_F$
4								GND			V_F	V_{CCH}	I_{11}	$.5 I_F$	
5				GND	V_R			GND				V_{CCH}	I_3		I_R
6	Note 2			GND		V_R		GND				V_{CCH}	I_4		I_R
7			I_{OL}					GND		GND		V_{CCL}	V_1		V_{OL}
8		GND	I_{OL}					GND				V_{CCL}	V_1		V_{OL}
9							I_{OL}	GND	V_{CCL}			V_{CCL}	V_6		V_{OL}
10			I_{OH}					GND	V_{CCL}			V_{CCL}	V_1	V_{OH}	
11							I_{OH}	GND		GND		V_{CCL}	V_6	V_{OH}	
12								GND	V_{CCH}	GND		V_{CCH}	I_9	I_{9K}	I_{9K}
13					GND	GND		GND	V_{PD}			V_{PD}	$I_9 + I_{14}$		I_{PDL}
14					GND	GND		GND				$V_{MAX.}$	I_{14}		$I_{MAX.}$
15	t_{pd} - Pin 1						See Test Circuit Below								50 nsec
16	t_{pd} + Pin 6						See Test Circuit Below								50 nsec
17	Pulse width Pin 1						See Test Circuit Below							90	160 nsec
18	Pulse width Pin 6						See Test Circuit Below							90	160 nsec

TABLE OF FORCING CONDITIONS

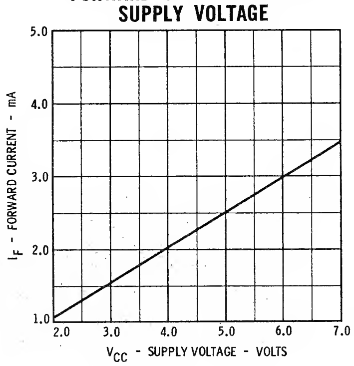
		-55°C	25°C	+125°C
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_{PD}	Volts		5.0	
V_{MAX}	Volts		8.0	
V_R	Volts		4.0	
V_F	Volts	0.0	0.0	0.0
I_{OL}	mA	15.0	15.0	14.0
I_{OH}	mA	-.18	-.18	-.18

TABLE OF TEST LIMITS

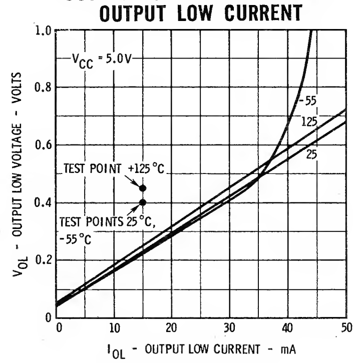
		-55°C Min.	-55°C Max.	25°C Min.	25°C Max.	+125°C Min.	+125°C Max.
$.5 I_F$	mA	-.80		-.80		-.75	
$2 I_F$	mA		-3.20		-3.20		-3.0
I_R	μA		5.0		5.0		10.0
V_{OL}	Volts		.40		.40		.45
V_{OH}	Volts	2.5		2.5		2.5	
I_{9K}	mA			.50	.75		
I_{PDL}	mA				9.0		
I_{MAX}	mA			to be supplied			

TYPICAL DC CHARACTERISTICS

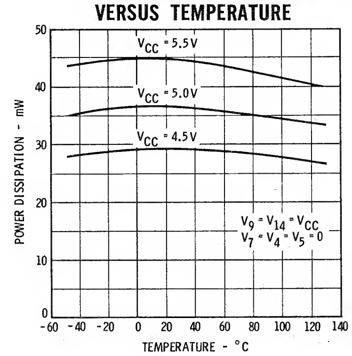
FORWARD CURRENT VERSUS SUPPLY VOLTAGE



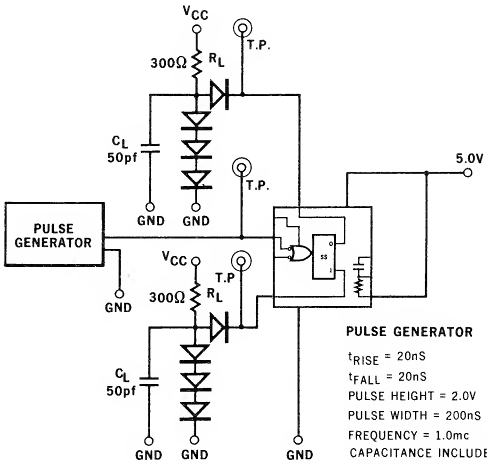
OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



TYPICAL POWER DISSIPATION VERSUS TEMPERATURE

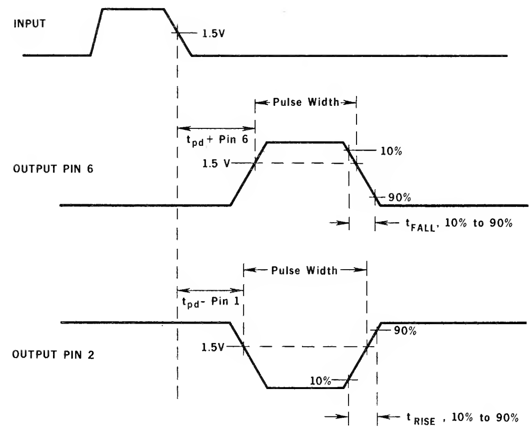


SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PULSE GENERATOR

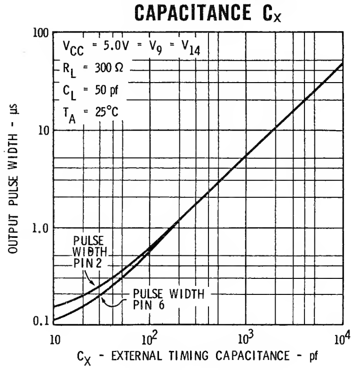
t_{RISE} = 20nS
t_{FALL} = 20nS
PULSE HEIGHT = 2.0V
PULSE WIDTH = 200nS
FREQUENCY = 1.0mc
CAPACITANCE INCLUDES PROBE AND JIG
ALL DIODES FD600



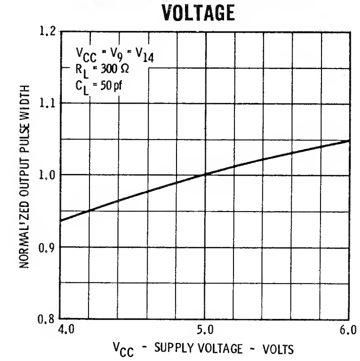
TIMING CHARACTERISTICS

(Test circuit above is used with appropriate modifications where necessary)

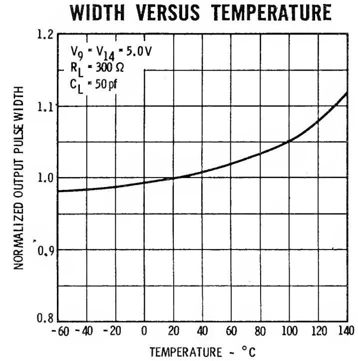
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



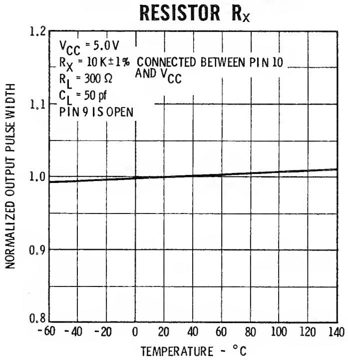
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



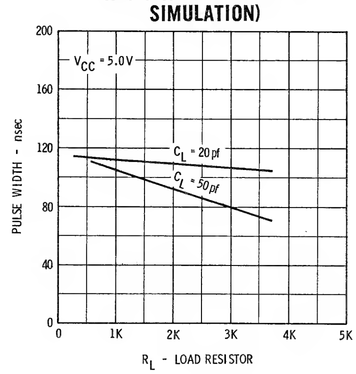
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



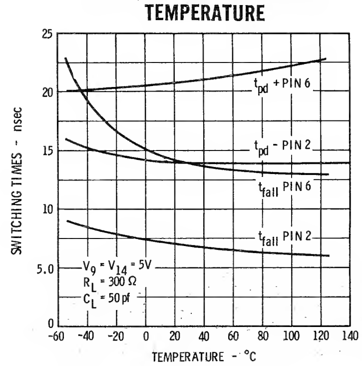
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



TYPICAL PIN 6 OUTPUT PULSE WIDTH VERSUS LOAD RESISTANCE (FAN-OUT SIMULATION)



SWITCHING TIMES VERSUS TEMPERATURE



RULES FOR USE OF DTμL 951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_x), the output pulse width is approximately 100 nsec.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_x) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_x + 20)$ with C_x in pf and T in nsec.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_x) of 9 KΩ minimum to 15 KΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5 R_x\ (C_x + 20)$ with R_x in KΩ, C_x in pf and T in nsec.
4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2-KΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 nsec for a 1.0-volt swing; 50 nsec for a 2.0 volt swing; 100 nsec for a 4.0 volt swing.
6. The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7. The minimum pulse width at output Pin 1 is approximately 100 nsec. This pulse width may be decreased to 50 nsec by connecting a 10-KΩ resistor between Pin 5 and V_{CC}.

USE OF DTμL 951 WITH MICROLOGIC AND MILLIWATT MICROLOGIC

The DTμL 951 may be operated from a V_{CC} supply of 4.0 to 6.6 volts. Operation is essentially independent of output resistive and capacitive loading. The input triggering action is initiated by a negative-going input with an amplitude change of 1.0 volt or more.

Micrologic or Milliwatt Micrologic outputs can drive the DTμL 951 input, provided the output swing is greater than 1.0 volt. Either of the outputs of the DTμL 951 can drive μL or MWμL inputs. Fan-out from DTμL 951 is 4 MWμL unit loads and 1 μL unit load, for DTμL 951 $V_{CC} \geq 4.0$ volts. Use of a resistor of 500 Ω to 1 KΩ from the DTμL 951 output to V_{CC} will increase fan-out into μL or MWμL.

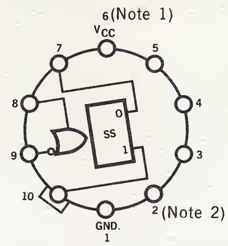
INPUT-OUTPUT LOAD FACTORS TO DTμL FAMILY

Each DTμL 951 input should be rated at 2 loads.

Each DTμL 951 output may drive 10 DTμL loads.

For input-output load factors of other DTμL elements, please refer to the DTμL Composite Data Sheet and to the individual DTμL element specifications.

TO-5 TYPE CONNECTION DIAGRAM (Top View)



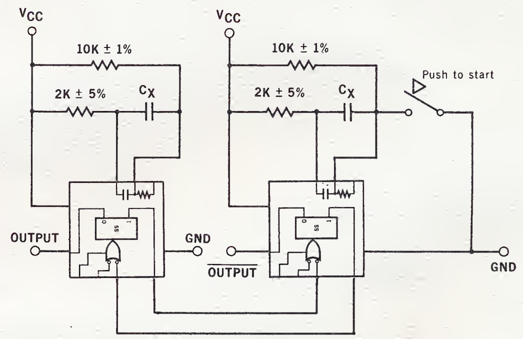
NOTES:

(1) The V_{CC} supply pin is not the tabbed pin on the DTμL 951.

(2) Connect to V_{CC} when R external is not used.

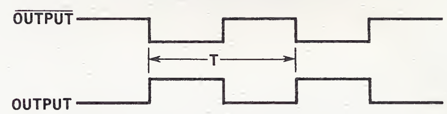
All data in this specification refers to 14-pin Cerpak pin numbers except this outline and the 10-pin reference numbers in the test sequence on Page 2.

STABLE MULTIVIBRATOR

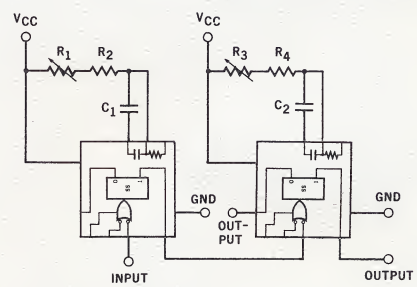


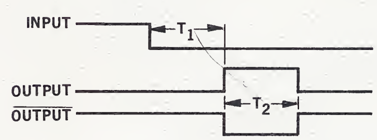
$$\frac{1}{f_{oscillation}} = T = \frac{(20+C_x)}{100} \text{ MICROSECONDS}$$

C_x IN PICOFARADS



VARIABLE DELAY PULSE GENERATION





Explanation

The input 951 determines T_1, the time before the initiation of the output pulse. The second or output 951 determines T_2, the output pulse width.

With $R_2 = 10\,K\Omega$ and R_1 a 5-KΩ potentiometer, T_1 is variable over a range of 2 to 3 and is given by $T_1 \approx 0.5\ (R_1 + R_2)\ (C_1 + 20\ \text{pf})$.

Similarly, with $R_4 = 10\,K\Omega$ and R_3 a 5-KΩ potentiometer, T_2 is $\approx 0.5\ (R_3 + R_4)\ (C_2 + 20\ \text{pf})$ and T_2 can be controlled by the potentiometer over a range of 2 to 3 since $10\,K\Omega \leq (R_3 + R_4) \leq 15\,K\Omega$.

A much greater range in T_1 and T_2 is available by varying C_1 and C_2.

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CTμL-952 THROUGH CTμL-957

FAIRCHILD PLANAR EPITAXIAL COMPLEMENTARY TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION - The Fairchild CTμL Family was designed for very high-speed, low-cost commercial systems applications. It features AND - OR - NOT logic.

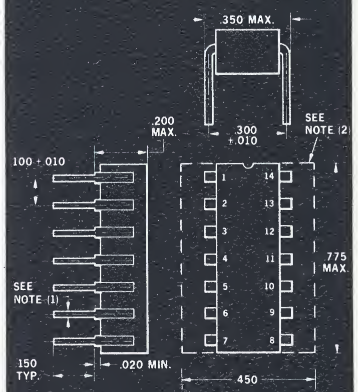
Using CTμL, the system designer can obtain average propagation delays per logic decision of 5 nsec, with associated rise times of 5 to 15 nsec. Binary counting rates of 30 Mc are typical. Special circuit design techniques have been used on CTμL to permit open transmission lines of 12-15 inches and still keep operation in the 5-nsec speed range. Logic swings are typically 3 volts. Noise margins are typically 0.5 volt or greater.

The system designer may use proven, low-cost, system fabrication techniques including two-sided printed circuit boards, simplified manual or automated insertion, flow-soldering attachment, "functional" printed circuit board layout and simple system heat removal schemes.

CTμL circuits are packaged in a ceramic package having short stiff leads in a dual in-line arrangement. CTμL circuits are designed to operate over a commercial ambient temperature range of +15 to +55°C. Power supplies are +4.5 V ±10% and -2 V ±10%. Power dissipation was designed to increase with fan-in and fan-out. Inverter Gates or AND Gates dissipate 30 to 35 mW nominally plus 5 mW per fan-out.

PHYSICAL DIMENSIONS

CTμL PACKAGE OUTLINE



NOTES:

1. Leads are a modified hexagon in cross section. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
2. Max. envelope for all planned packages of this design family.

THE COMPLEMENTARY TRANSISTOR MICROLOGIC FAMILY:

CTμL-952 —Dual 2-Input Inverter Gate (two circuits in one package). This element is used mainly for voltage level setting and logic inversion. Its high level output is regulated for voltage and temperature to track the input "turn-on" threshold of other inverter gates. The output may be tied to any other output in the CTμL family to perform the OR function. Average propagation delay is typically 9 to 12 nsec.

CTμL-953 —2-2-3-Input AND Gate (three gates in one package).

CTμL-954 —Dual 4-Input AND Gate (two gates in one package).

CTμL-955 —8-Input AND Gate with two outputs. The AND Gates (953, 954, 955) are non-inverting, non-saturating, PNP-NPN, cascade-connected emitter-followers. The 955 element has two separate outputs that may be used to isolate the output logic signal. Any AND Gate output may be OR tied to any other outputs in the CTμL family. Average propagation delay of the AND Gates is 2.7 to 4 nsec, depending on loading.

CTμL-956 —Dual 2-Input Buffer (two buffers in one package). The Buffer is a non-inverting, level setting circuit intended to drive high fan-outs. It may also be used as a line-driver. Average propagation delay is typically 12 to 15 nsec.

CTμL-957 —Dual-Rank Flip-Flop. This is a multi-purpose, directly-coupled, dual-rank flip-flop useful for counters, registers and other "storage" applications. Outputs of the 957 provide voltage levels identical to the 952 Inverter Gate Output. Through delay from the blocking inputs going negative to (1) the output going positive is typically 15 nsec and (2) the other output going negative, is 20 nsec. Minimum data input pulse width is typically 12 nsec.

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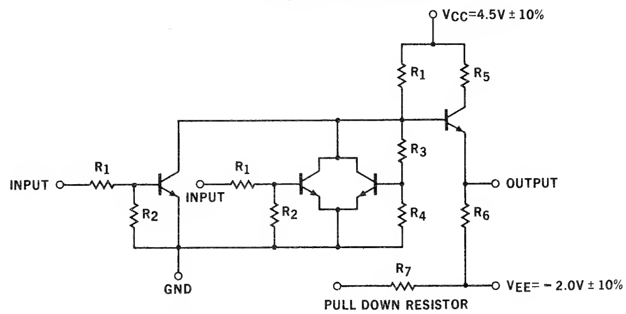
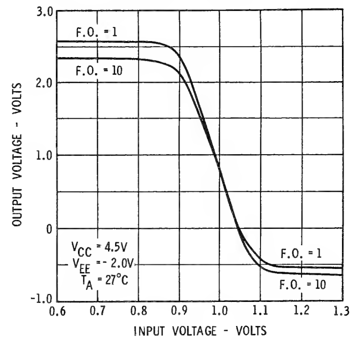
CTμL-952 DUAL 2-INPUT INVERTER GATE

CIRCUIT DIAGRAM

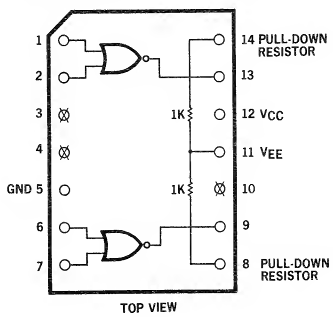


NOTE: ONLY ONE 2-INPUT INVERTER GATE SHOWN

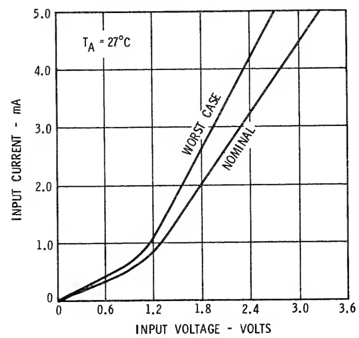
TYPICAL TRANSFER CHARACTERISTICS



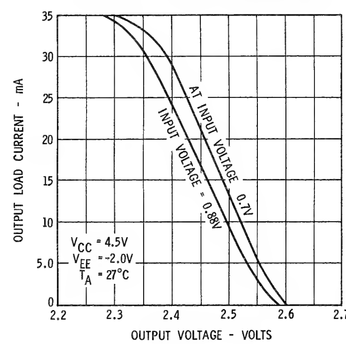
LOGIC DIAGRAM (POSITIVE LOGIC)



INPUT CHARACTERISTICS

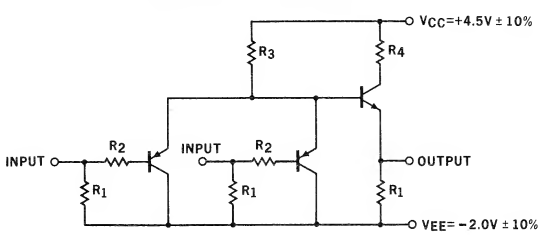


TYPICAL HIGH-LEVEL OUTPUT CHARACTERISTICS



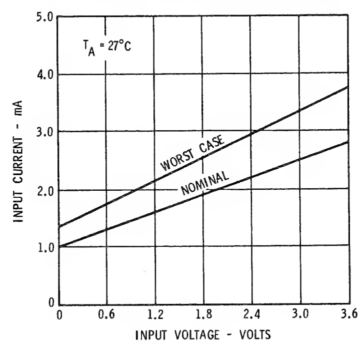
CTμL-953, 954, 955 AND GATES

TYPICAL CIRCUIT DIAGRAM

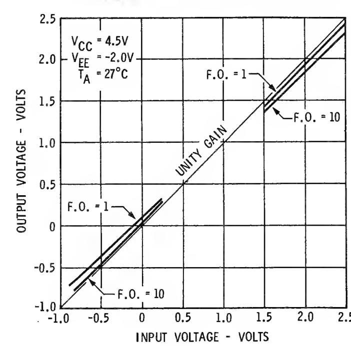


NOTE: ONLY ONE 2-INPUT GATE SHOWN

INPUT CHARACTERISTICS

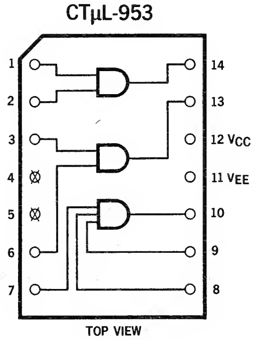


TYPICAL TRANSFER CHARACTERISTICS

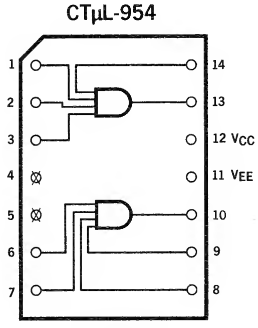


LOGIC DIAGRAMS (POSITIVE LOGIC)

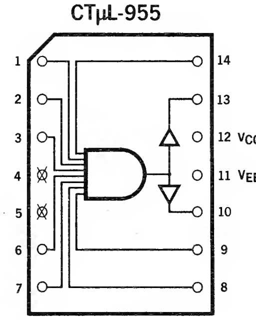
CTμL-953



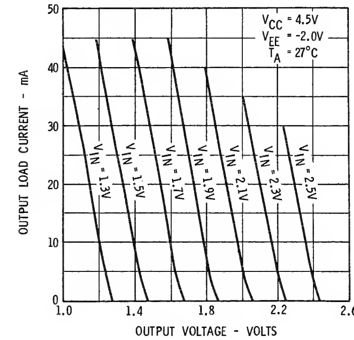
CTμL-954



CTμL-955

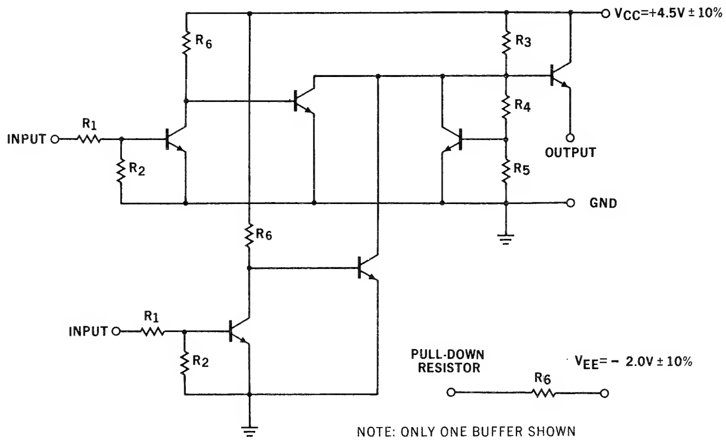


TYPICAL OUTPUT CHARACTERISTICS



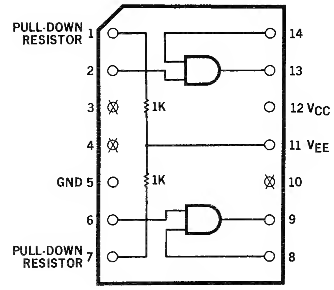
NOTE: ⊗ = PIN NOT USED

CTμL-956 BUFFER CIRCUIT DIAGRAM



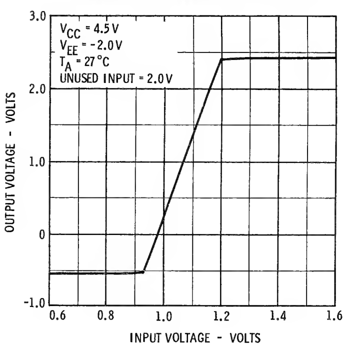
NOTE: ONLY ONE BUFFER SHOWN

CTμL-956 LOGIC DIAGRAM (POSITIVE LOGIC)

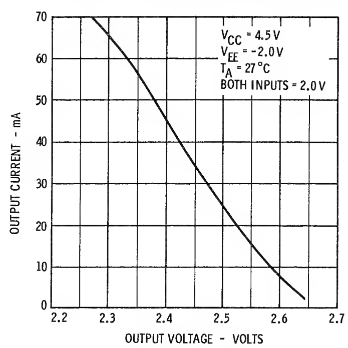


TOP VIEW

CTμL-956 TYPICAL TRANSFER CHARACTERISTICS

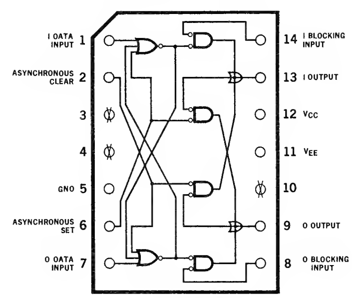


CTμL-956 TYPICAL HIGH-LEVEL OUTPUT CHARACTERISTICS



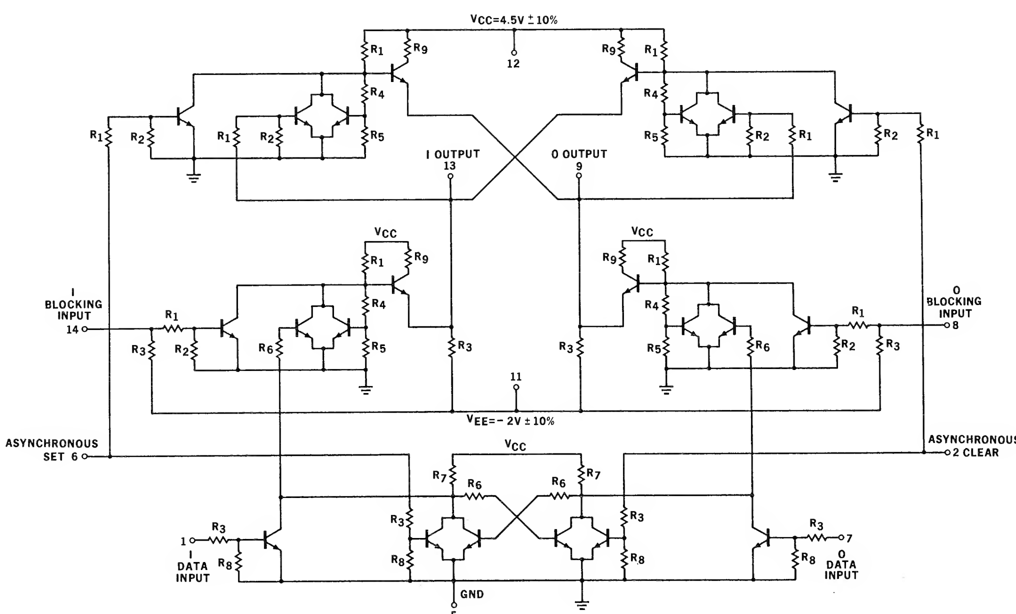
(INPUT CHARACTERISTICS SAME AS CTμL-952)

CTμL-957 LOGIC DIAGRAM (POSITIVE LOGIC)



TOP VIEW

CTμL-957 DUAL-RANK FLIP-FLOP CIRCUIT DIAGRAM



NOTE: ⊗ = PIN NOT USED

AND-OR LOGIC: Greatest system speed will be realized by performing most of the logic with the AND Gates ("AND"ing with the inputs, "OR"ing with the outputs). After several levels of this, the slower Inverters or Buffers may be used to re-establish noise immunity levels.

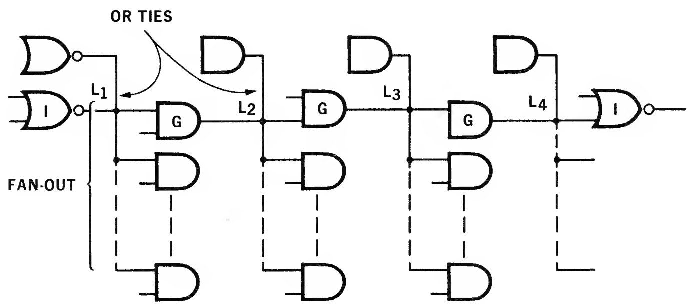
CTμL NORMALIZED LOADING CHART

ELEMENT	INPUT	MAX. OUTPUT
952	1.5	12
953	1	15
954	1	15
955	1	Sum of both outputs = 15
956	1.5	25 (or for 50Ω line: 68Ω to GND with F.O. = 10 AND gates)

ELEMENT	DATA INPUT	BLOCKING GATE INPUT	ASYNCHRONOUS INPUT	OUTPUT
957	1	3.5	2	9.5

LEVEL RESETTING: There is signal level degradation going through an AND Gate; therefore, signal level must be restored after going through several cascaded gates. This may be accomplished by using either the 952 Inverter Gate, the 956 Buffer, or by driving the 957 Flip-Flop. The purpose of the following loading rules is to guarantee a worst case noise immunity at L_4 of 250 mV.

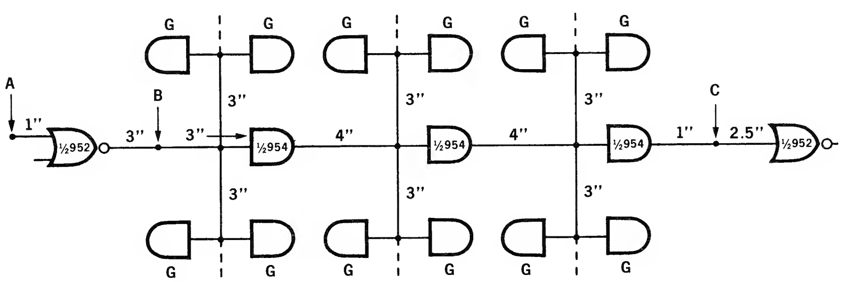
LOADING RULES: For the case of Three Cascaded AND Gate Levels



NOTES:

1. Loads and OR Ties at L1 + L2 + L3 + L4 ≤ 45.
2. Maximum Loading at L1 = 12, L2 = 15, L3 = 15, L4 = 15.
3. Both Rules 1 and 2 Must be Satisfied Simultaneously.

PROPAGATION DELAY TEST SET-UP

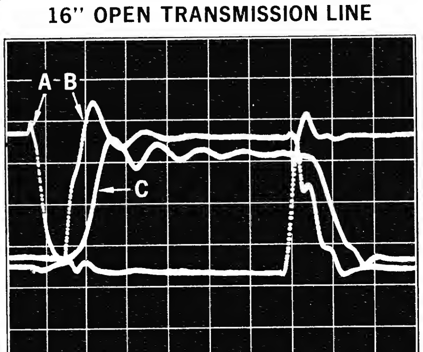


NOTES:

1. Above configuration may have as many as 8 logic levels for an average propagation delay of 2.6 to 3.1 nsec per logic decision.
2. t_{pd} measurements taken at +0.96V.

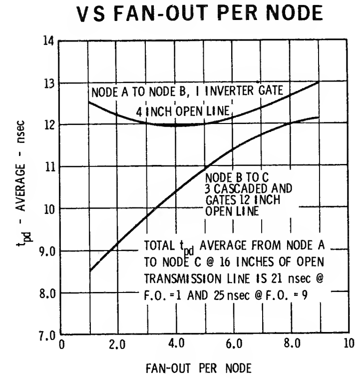
t_{pd} WAVEFORMS AT FAN-OUT = 5 PER NODE, 16" OPEN TRANSMISSION LINE

VERT = 1.0 V cm



HORIZ = 20 nsec / cm

TYPICAL PROPAGATION DELAY OF AN INVERTER DRIVING 3 CASCADED AND GATES VS FAN-OUT PER NODE



CTμL 957 DUAL-RANK FLIP-FLOP

The CTμL 957 is a dual-rank directly-coupled Flip-Flop. The first rank or "master" consists of two cross-coupled NOR gates similar to the CTμL 952. The second rank or "slave" employs OR ties as shown in the functional logic diagram of Fig. 1, thereby minimizing through delay. Two NAND gates provide feedback inversion, while the other two provide gating between "master" and "slave."

The primary data inputs to the Flip-Flop are through pins 1 and 7. These inputs work directly from AND gate outputs, allowing OR ties and multiple inputs to each Flip-Flop (see Fig. 2).

To take advantage of the dual-rank principle, mutually exclusive active inputs should be applied to the gating to "master" and "slave" so that only one or the other can change at any particular instant. This is easily accomplished in the CTμL 957 due to the difference in active polarity of the two gates. Thus, what appears as a logic 1 to CTμL gates of the Flip-Flop data inputs is a logic 0 to the "slave" gates, and vice versa.

These observations lead to the connection of pin 1 to pin 14 and pin 7 to pin 8 as shown in Fig. 2. Although both "slave" gates are not necessarily inhibited when a change takes place, the output cannot change unless both data inputs are logic 0. Therefore, this connection is the usual one, tending to minimize the loading of timing circuits.

In case phased timing signals are advantageous, pins 8 and 14 may be used independently as long as they are never active (low) while their corresponding data inputs are high.

Direct inputs to both "master" and "slave" appear on pins 2 and 6. A logic 1 (high) on either input sets or resets the "master" and simultaneously inhibits a feedback NAND gate in the "slave." The net effect is that both "master" and "slave" move to the desired condition during the presence of the direct input signal.

The response of the Flip-Flop to concurrent inputs tending to set opposite output conditions is ambiguous. That is, simultaneous logic 1 inputs must be avoided for well-defined operation.

FIG. 1. DUAL-RANK FLIP-FLOP

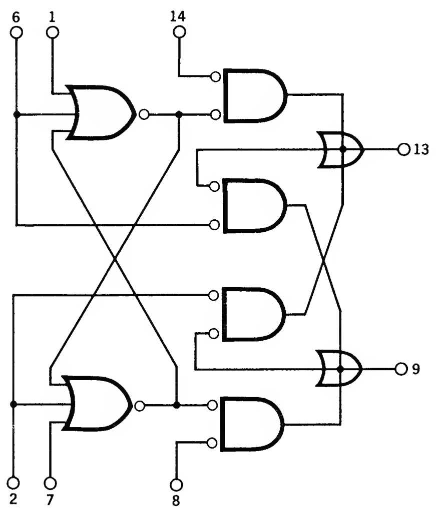
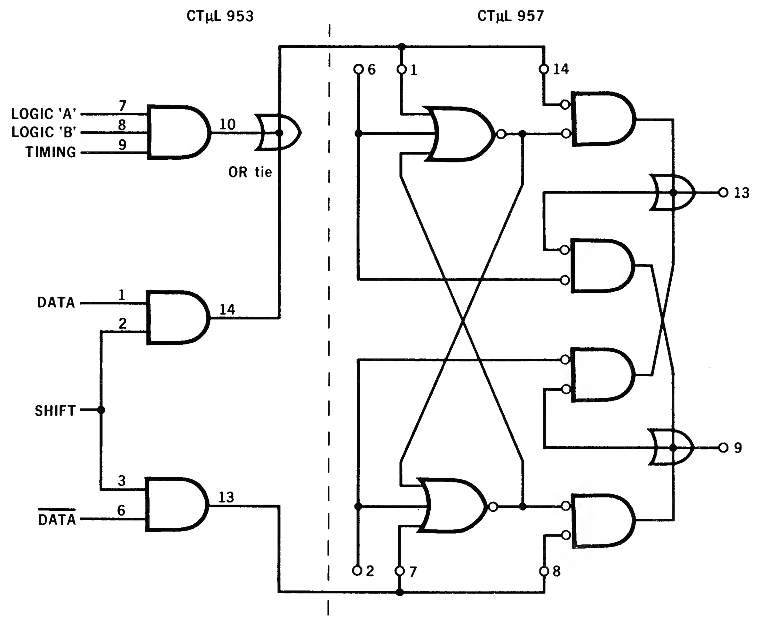


FIG. 2. TYPICAL FLIP-FLOP GATING



"OR" TIES

All CTμL circuits have provision for output OR ties. In each of these circuits the base-emitter diode of the output transistor isolates the output from the input logic-node. Therefore, if several outputs are tied together, the output of the whole will seek the level of the most positive logic-node without disturbing the others. Along with the output emitter resistors, tied outputs are analogous with conventional diode OR circuits. An OR tie is symbolized by enclosing the tie point with a small logic OR symbol (see Fig. 2).

Each OR tie parallels two or more emitter resistors, reducing the total output current. Taking the fan-out capability of the lowest rated output in an OR tie as a starting point, each OR-tied output reduces the fan-out capability by one (for an N-way OR tie, fan-out capability must be reduced N-1). The most restrictive OR tie involves a Flip-Flop output, but there seems to be no practical use for such an application. OR-tied buffers lose their load factor advantage when other units are involved, so that buffers should only OR tie to other buffers.

UNCOMMITTED INPUTS

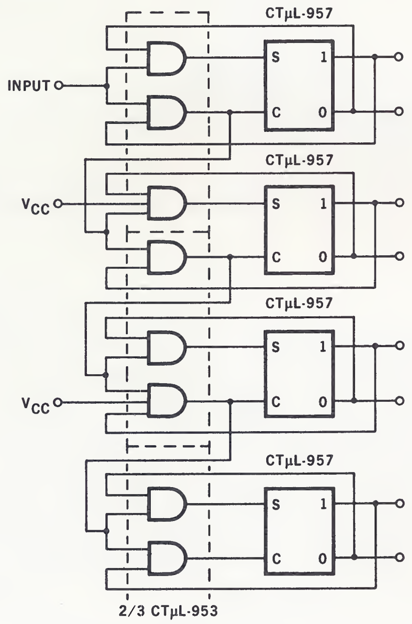
Open inputs to the CTμL 953, 954, 955 Gates and of the CTμL 956 Buffer are equivalent to logic zeros and effectively inhibit the device outputs. When the fan-in of these units is not fully used, spare inputs should be treated as follows:

1. CTμL 953, 954, 955 - Return to positive supply. Parallel companion inputs to the same logic output should be avoided.
2. CTμL 956 - Return to positive supply through 1000 Ω resistor, or connect both companion inputs to the same logic output.

PULLDOWN RESISTORS

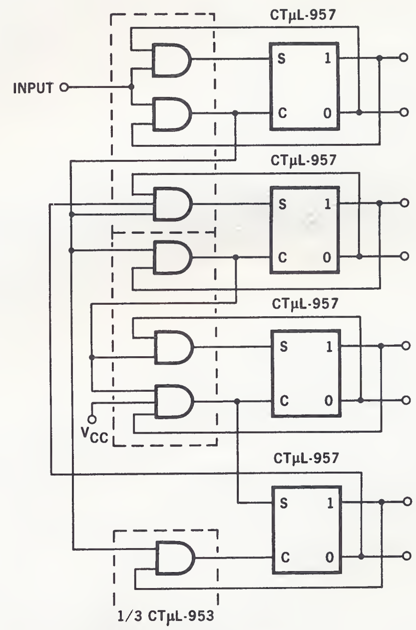
Whenever 952 Inverter Gates or 956 Buffers constitute the only loading of an output, minimum fall-time delay will not be realized unless pull-down resistors are connected to the inputs. These resistors are included in the 952 and 956 packages. One resistor suffices for each two inputs. Pulldown resistors are not needed when two or more Gate inputs or outputs are connected to the same node as a 952 or 956 input.

FIG. 3. CTμL SERIAL BINARY COUNTER



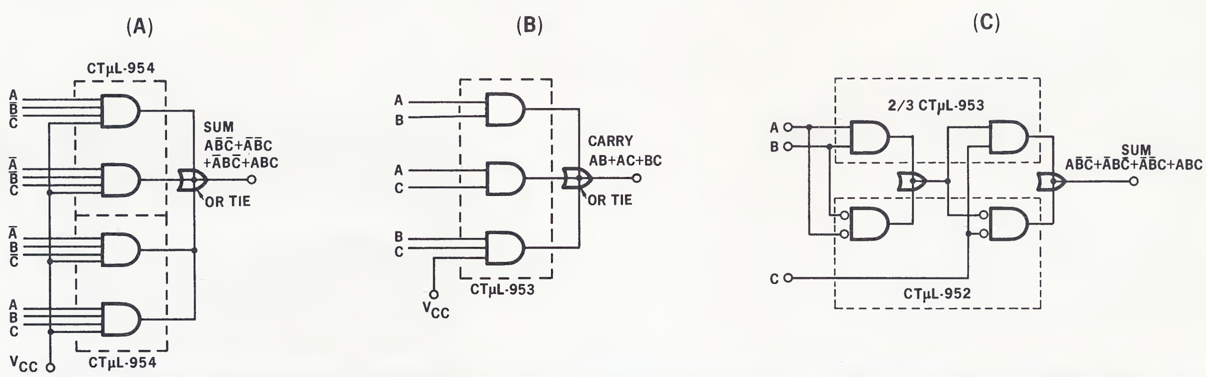
NOTES:
1. On all CTμL-957'S, tie pins 1-14 and 7-8.
2. All gates are CTμL-953'S.

FIG. 4. CTμL 1-2-4-8 DECADE



NOTES:
1. On all CTμL-957'S, tie pins 1-14 and 7-8.
2. All gates are CTμL-953'S.

FIG. 5. HIGH-SPEED ADDER



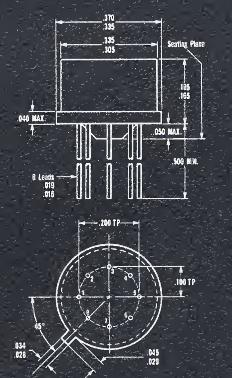
CμL 958
DECADE COUNTER
DIFFUSED PLANAR EPITAXIAL MICROLOGIC

GENERAL DESCRIPTION - The CμL 958 is a complete Decade Counter consisting of four cascaded binary triggered flip-flops modified by a feedback loop to count in the familiar 8-4-2-1 code. Provision is made for clearing and presetting any one of the possible decimal states. The monolithic structure employs only resistors and transistors and is manufactured with Fairchild Planar Epitaxial process to assure maximum performance and reliability.

The Decade Counter is designed for a nominal power supply voltage V_{CC} of 3.6 to 4.0 volts loaded by CμL 959 or MWμL in the temperature range from 0°C to +75°C.

At 0°C V_{CC}(min) = 3.6 volts and at 75°C V_{CC}(max) = 4.2 volts.

PHYSICAL DIMENSIONS
(SIMILAR TO TO-5)



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated kovar
Weight: 1.12 grams

(PRODUCT CODE: UX5995829X)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	-55°C to +150°C
Voltage at pin 7 (0°C to +75°C)	+6.0 V
Count Input Pin Voltage	+4.0 V, -2.0 V
Reset Input Pin Voltage	+4.0 V, -2.0 V
Current into Each Output Terminal	±5.0 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Parameter	Min.	Typ.	Max.	Units	Conditions
Count Input-Low			0.45	V	
Count Input-High	1.2			V	
Count Input Pulse Width-High	150			nsec	
Count Input Slope-Positive Going	1.0			V/μsec	
Maximum Count Input Frequency			2.0	Mc	
Reset Input-Low			0.45	V	
Reset Input-High	1.2			V	
Output-Low			0.35	V	I_{OUT} = 0.4 mA V_{CC} = 4.0 V
Output-High	1.4			V	I_{OUT} = -0.7 mA V_{CC} = 3.6 V
Power Consumption		135		mW	V_{CC} = 3.8 V

NOTE:

(1) These ratings are limiting values above which serviceability of unit may be impaired.

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Count Input Impedance: 2 KΩ in series with a transistor base-emitter diode

Reset Input Impedance: 300 Ω in series with a transistor base-emitter diode

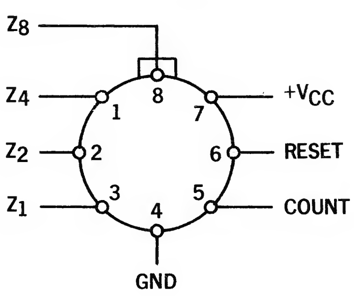
Maximum Delay from Count Input to Z_8 Output (count 7 to 8): 300 nsec (Load: 2 KΩ parallel with 50 pf from each output to ground)

The circuit is reset to count 0 (all outputs high) with a high level at the reset input pin.

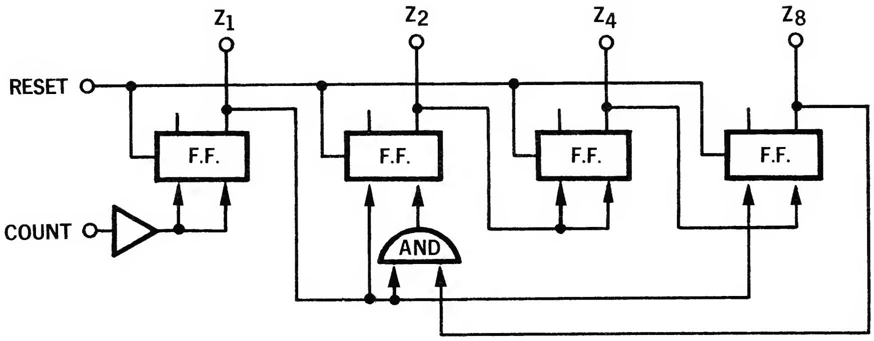
To preset an arbitrary count: 1) reset to count 0 and then return the reset pin to a low level; 2) ground (below 0.45 V) the appropriate outputs.

TO-5 CONNECTION DIAGRAM

(Top View)



BLOCK DIAGRAM



OUTPUT WAVEFORMS

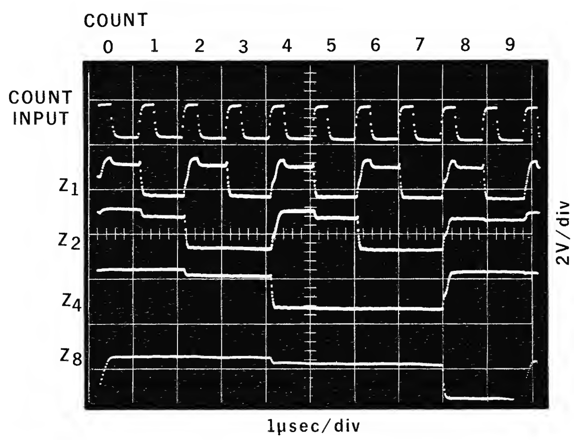


TABLE OF OUTPUT STATES

COUNT (H=High, L=Low)

	0	1	2	3	4	5	6	7	8	9
Z_1	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H
Z_4	H	H	H	H	L	L	L	L	H	H
Z_8	H	H	H	H	H	H	H	H	L	L

DTμL 962

TRIPLE THREE-INPUT GATE ELEMENT

FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION - The DTμL 962 Element consists of three 3-Input Gates on a monolithic chip. The circuit design and fabrication technology are matched identically to the DTμL 930 Dual 4-Input Gate Element and to the DTμL family in general.

The logic gating sections of a computer or data handling system may be economically generated from the DTμL family with these elements:

DTμL 946 Quad 2-Input Gate Element—inverters, exclusive "OR's", fan-in 2 gates.

DTμL 962 Triple 3-Input Gate Element—fan-in 3 gates.

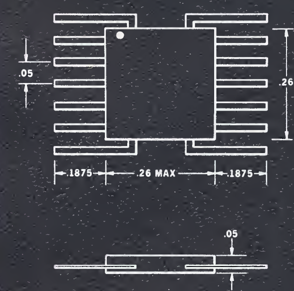
DTμL 930 Dual 4-Input Gate Element—higher fan-in gating (with input extension available in each gate).

DTμL 933 Dual 4-Input Extender Element—for fan-in extending.

DTμL 932 Dual Buffer Element—for high fan-out, good capacitive drive capability, and interface driving. The 932 fan-in may also be increased by use of 933 Elements.

Refer to the DTμL 931 and DTμL 945/948 Clocked Flip-Flop Element specifications for the storage function, to the DTμL 951 for a compatible monostable multivibrator function, and to the DTμL Composite specification for complete test data and additional characteristic data.

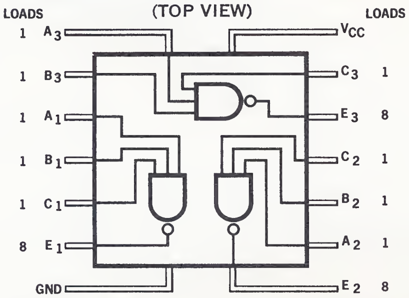
PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



PART NO. UX3996251X

LOGIC DIAGRAM AND LOAD FACTORS

(TOP VIEW)

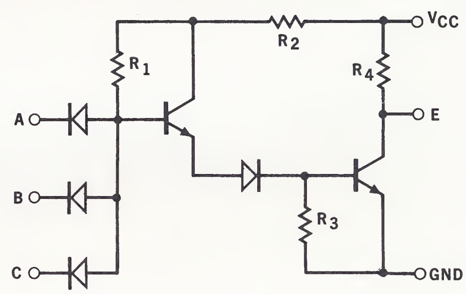


SCHEMATIC DIAGRAM

(ONE GATE ONLY)

TYPICAL RESISTOR VALUES

$R_1 = 2.00K\Omega$
$R_2 = 1.75K\Omega$
$R_3 = 5.00K\Omega$
$R_4 = 6.00K\Omega$



TEST SPECIFICATIONS AND CHARACTERISTIC CURVES

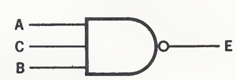
CHARACTERISTICS - All curves and other data shown in the DTμL 930 Element specifications and in the DTμL Composite specifications apply equally to each gate on the DTμL 962 Element, except as it may be necessary to modify test circuits to fit the proper pin configurations.

TEST SPECIFICATIONS - The test sequence for the DTμL 930 Element, shown on Page 2 of the DTμL Composite specification, and the various tables of test conditions, test limits, LTPD's, and t_{switch} conditions from Pages 3 and 5 also apply to the 962 Element, except as modified below:

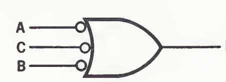
1. Test limits for I_{PDH} and I(max) are 1.5 times the 930 values.
2. Ignore all tests relating to pins D, X, and Y.
3. Use a t_{pd} test circuit similar to the DTμL 930 with gate 3 driving gate 2.

LOGIC FUNCTIONS

POSITIVE (NAND) LOGIC $E=\overline{A \cdot B \cdot C}$



NEGATIVE (NOR) LOGIC $E=\overline{A+B+C}$



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